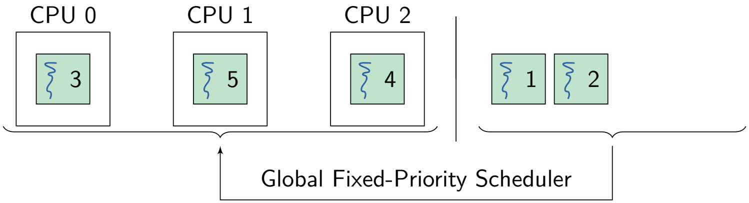
InterSloth: Global Hardware-Based Scheduling in a MultiCore-RTOS on RISC-V

Christian Dietrich

2019-09-24

Fixed-Priority Real-Time Scheduling

- Schedule Threads according to a Fixed Priority onto Processor(s)
  - Optimal priority assignments for unicore ({rate,deadline} monotonic)
  - For multicore: Global fixed-priority is most flexible schema



- Real-time analysts would like a zero RTOS overhead, but…
  - Global scheduling requires global synchronization (locking)
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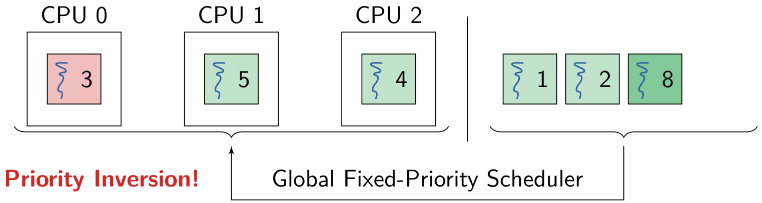

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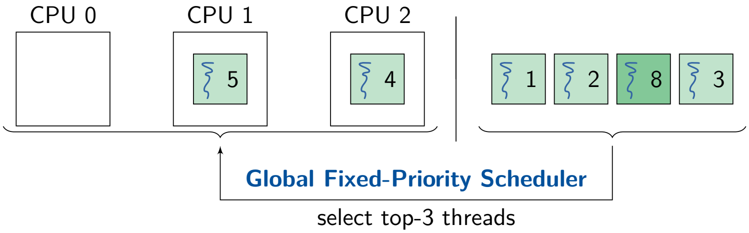

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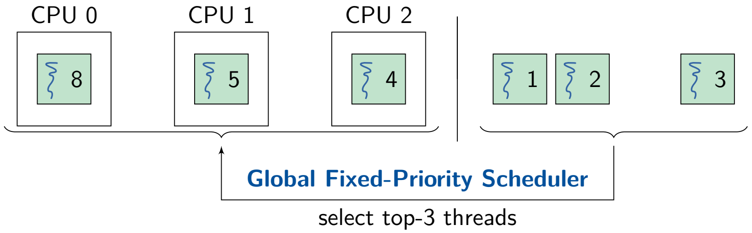

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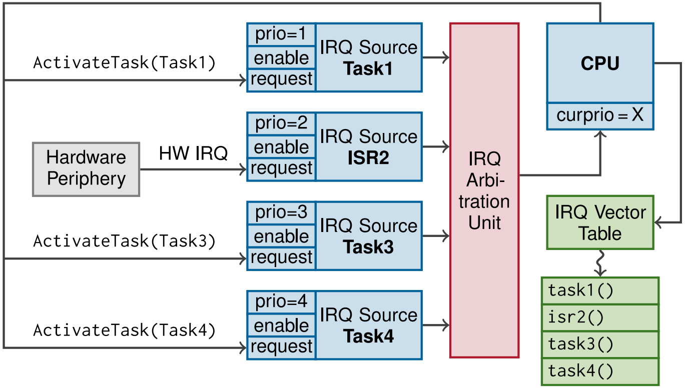
Sloth: Threads as Interrupts

[Hof+09; HLSP11; Hof+12] [Dan+14; Mül+14]

- Sloth RTOS in a Nutshell: Threads $\equiv$ ISR
  - Interrupt controller already selects high-prio interrupt source.
  - Interrupt service routine performs context switch between threads.
  - Supports only unicore and partitioned multicore scheduling.



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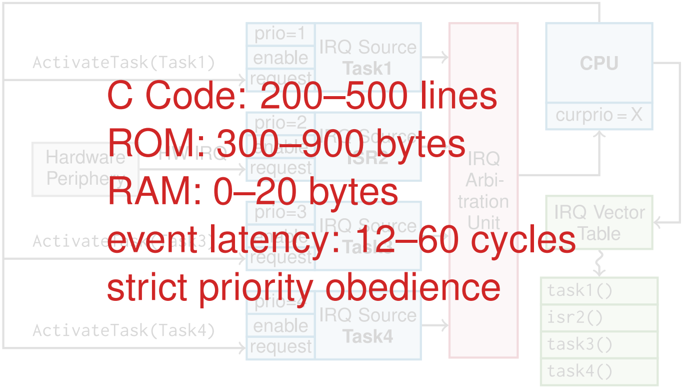


C Code: 200–500 lines

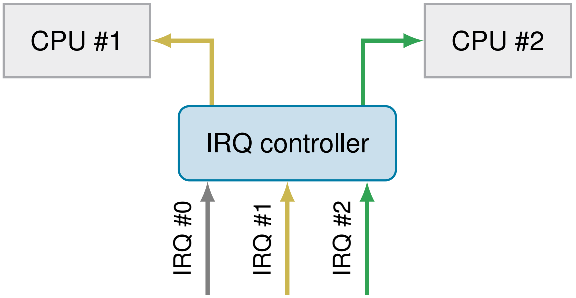
ROM: 300–900 bytes

RAM: 0–20 bytes

event latency: 12–60 cycles

strict priority obedience

InterSloth: Extension to Global FP Scheduling



- We require a strict priority-obedient IRQ controller, but existing…
  - …use a threshold and choose at random (ARM)
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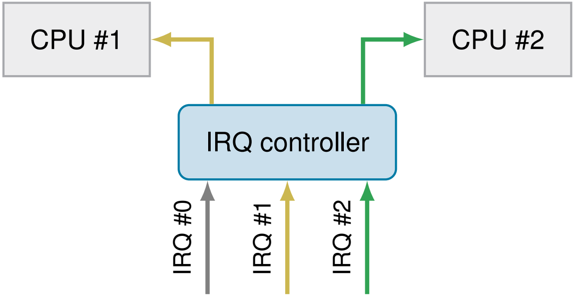

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MIRQ-V: A Strict Priority-Obedient Multi-Core IRQ Controller

Motivation

MIRQ-V: A Strict Priority-Obedient Multi-Core IRQ Controller

InterSloth: An RTOS on Top of MIRQ-V

Evaluation

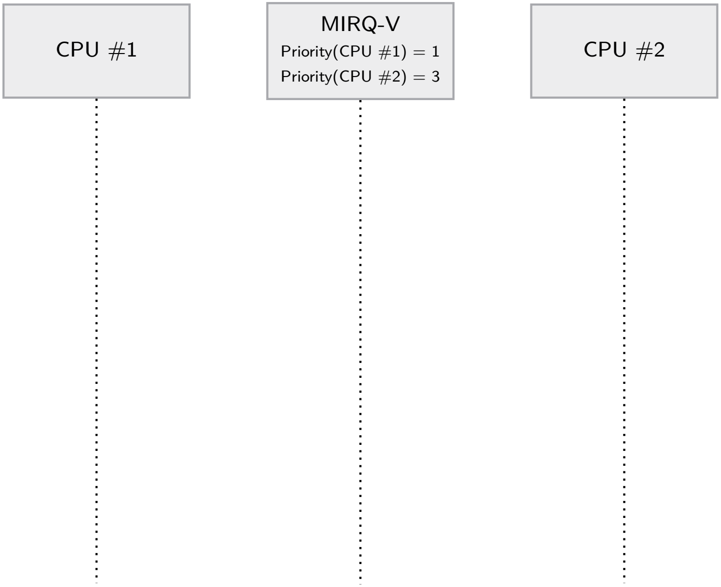
Conclusion

MIRQ-V: Features and Rocket Integration

- Feature set is designed for hard real-time systems
  - Freely configurable interrupt and CPU interfaces
  - Up to 255 interrupt/CPU priority levels
  - Highest-priority IRQ is always delivered to lowest-priority CPU
  - Software-triggered IRQ sources and IRQ migration

- Integration with a RISC-V processor
  - Rocket Chip Generator is written in Chisel HDL (Scala DSL)
  - MIRQ-V replaces the *Platform-Level Interrupt Controller* (PLIC)
  - Existing prototype and work on a more efficient implementation

Example Interrupt Delivery with Software IRQ



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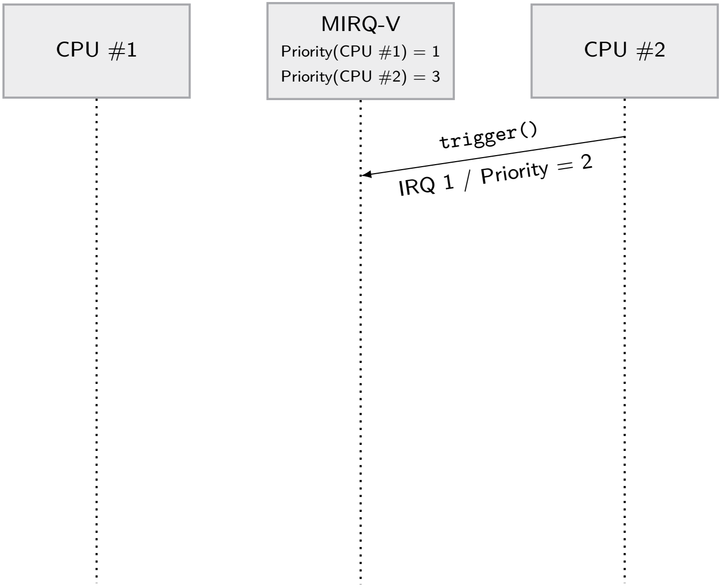

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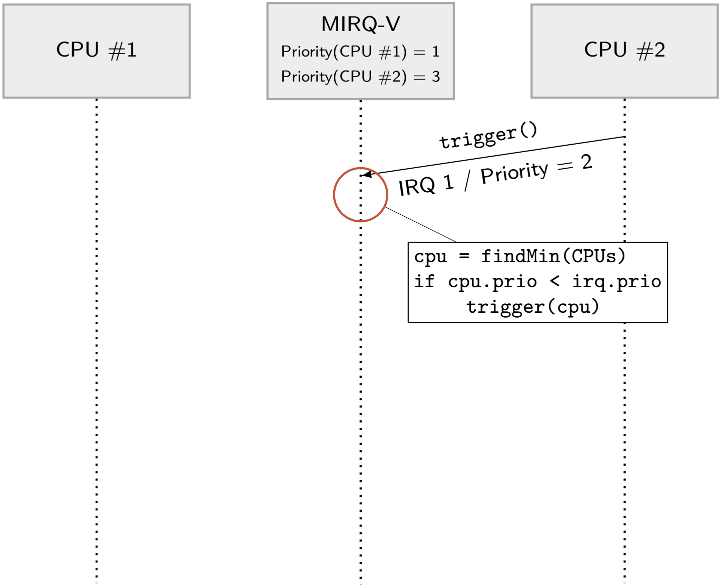

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cpu = findMin(CPUs)
if cpu.prio < irq.prio
    trigger(cpu)
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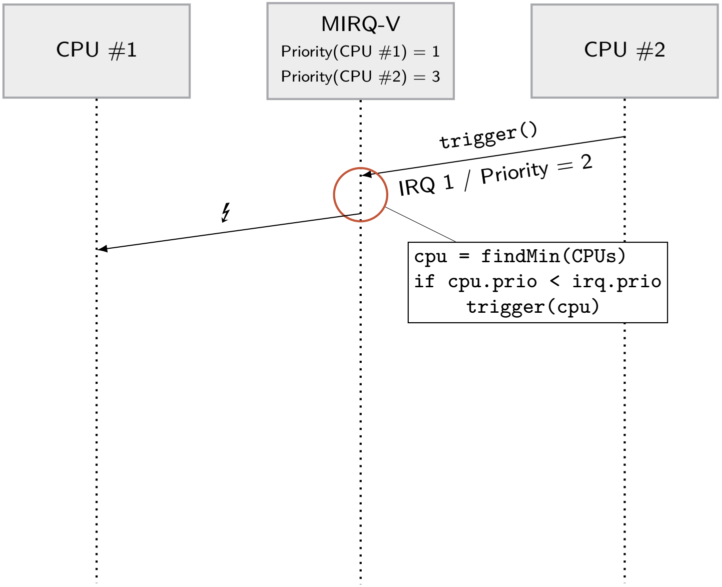

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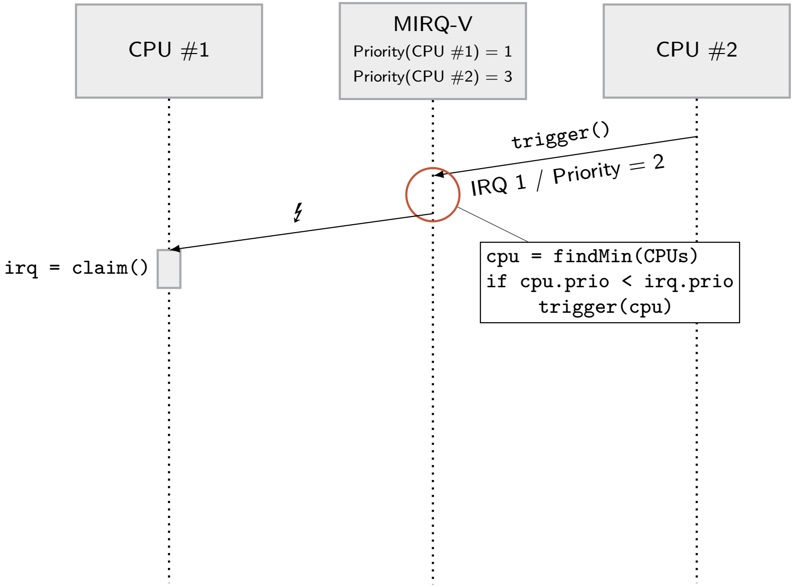

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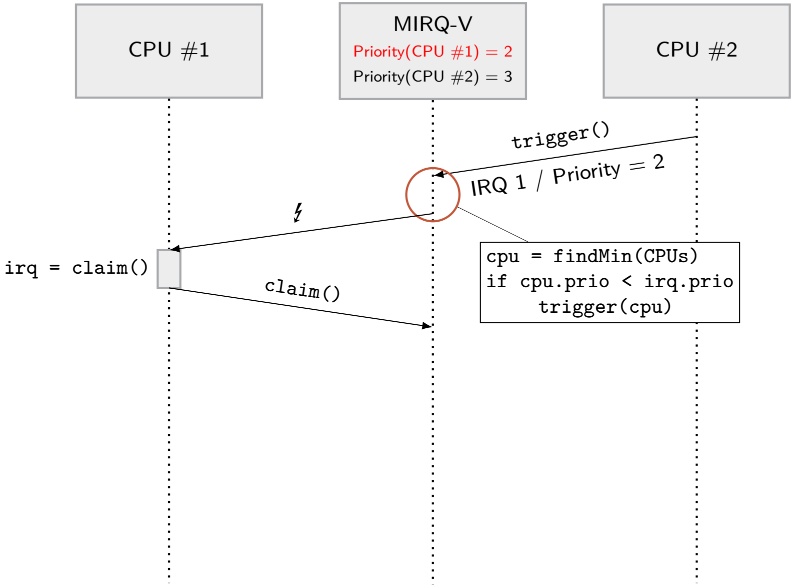

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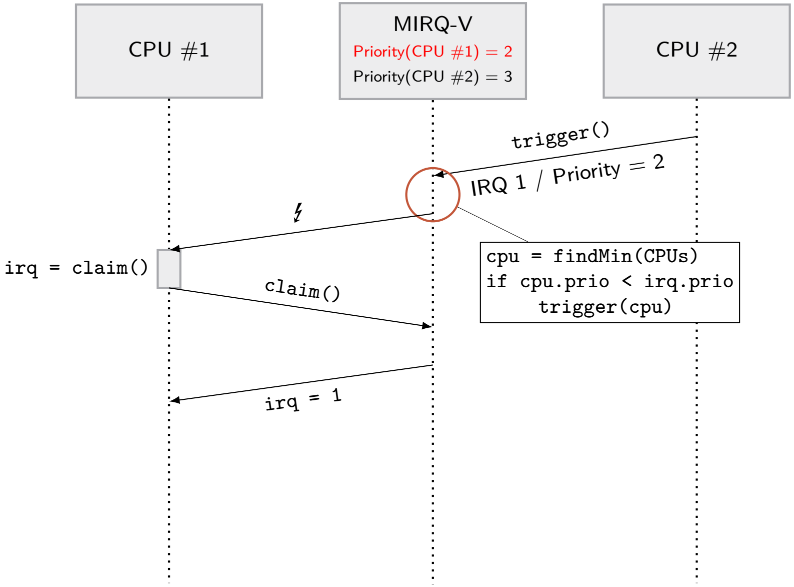

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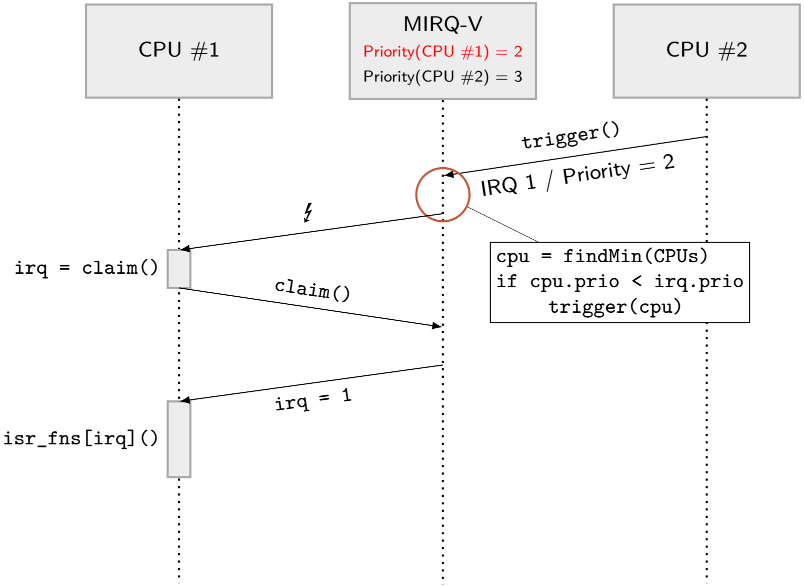

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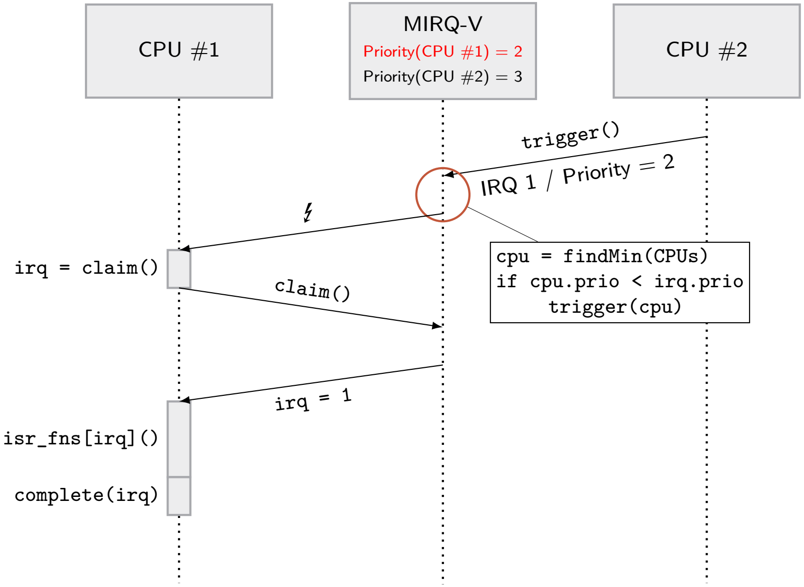

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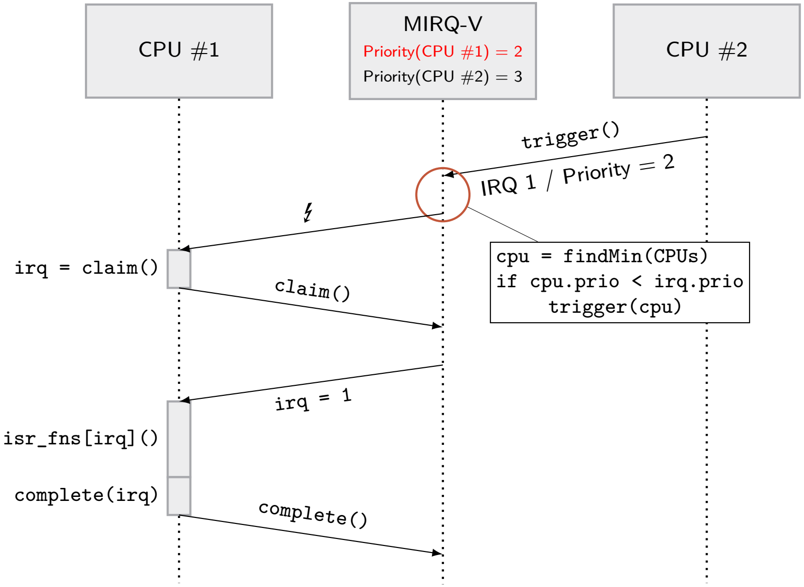

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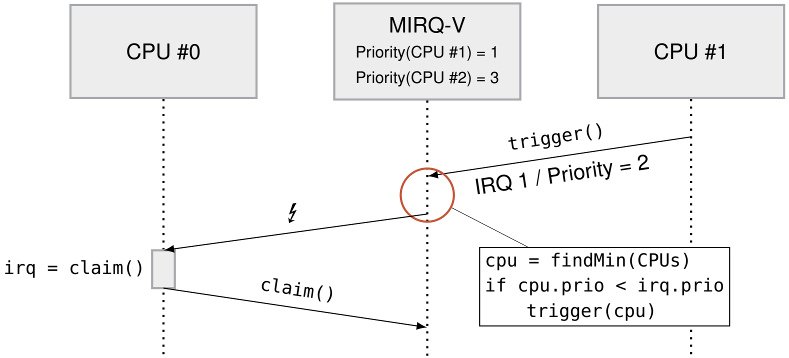
MIRQ-V: A few technical details

- Race conditions between delivery and CPU-priority changes
  - Normal PLIC IRQ Source has two states: *pending* and *in service*
  - Introduce *delivered* if CPU is informed but has not `claim()`ed.
  - Automatic re-delivery of delivered IRQs if a CPU priority changes.



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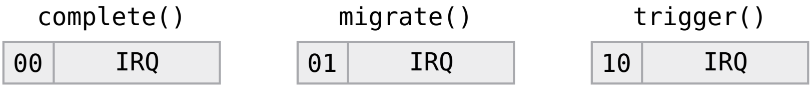
- Backward Compatibility with the original PLIC
  - `migrate()` IRQ to other CPU, `trigger()` from software.
  - Encode new commands into `claim/complete`-register values



Motivation

MIRQ-V: A Strict Priority-Obedient Multi-Core IRQ Controller

InterSloth: An RTOS on Top of MIRQ-V

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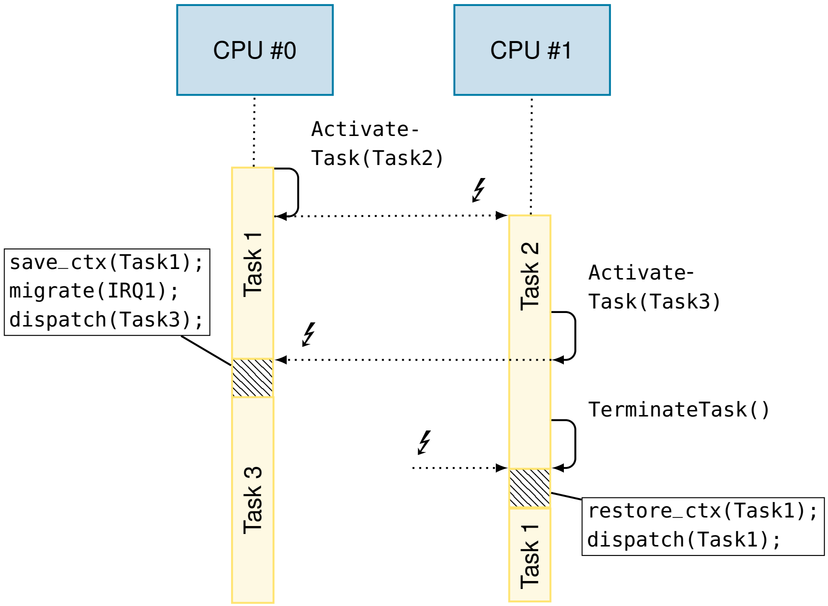
InterSloth: An RTOS for MIRQ-V

- MIRQ-V already performs most of the heavy lifting
  - No global synchronization need, as MIRQ-V is single source of truth.
  - Scheduling and re-scheduling decisions are calculated in parallel.
  - The CPU with the lowest priority is informed about high-priority IRQ.

- InterSloth must handle preemption of already running ISRs
  Remember: Sloth $\Rightarrow$ Thread $\equiv$ ISR
  - Preemption can happen at any time and must be performed transparent.
  - ISR prologue always safes old thread context.
  - Start new thread or resume to old thread context.

Example of Thread Activation and Preemption



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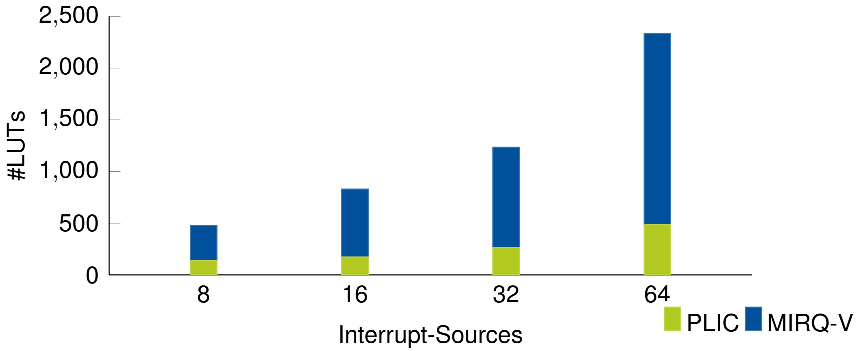
Evaluation: MIRQ-V

- IRQ arbitration in 1 cycle, delivery in 4 cycles
- MIRQ-V Design with parametrizable number of IRQs/CPUs
  - LUT demand is linearly larger than PLIC LUT demand
  - Full Rocket Chip uses 23.000 LUTs



Evaluation: InterSloth

- Cycle-Accurate Simulator on Verilog level (Verilator)
  - Timing Measurements from Software with RISC-V's `mcycle` register
  - Measure time that is spent in the InterrSloth kernel

- Measure three characteristic InterSloth system calls
  - Context switch must save and restore 32 general-purpose registers.

System Call	Cycles	Instructions
`ActivateTask()` *Trigger thread and dispatch on different CPU*	318	130
`TerminateTask()` *Start the idle thread*	93	60
`ChainTask()` *Destroy current thread and dispatch in this CPU*	261	148

Conclusion

- Problems for Multi-Core Real-Time Scheduling
  - Overheads for Inter-Core Communication and Synchronization
  - Multi-Core IRQ Controllers are not strictly enforcing priorities.
- MIRQ-V: A Strict Priority-Obedient Multi-Core IRQ Controller
  - Always route highest-priority IRQ to lowest-priority CPU.
  - Parametrizable Hardware Design with Rocket (RISC-V) Integration
  - Software-Triggered IRQs and IRQ Migration
- InterSloth: Minimal-Effort Global Fixed-Priority Scheduling
  - ISRs save the old and restore/start the new thread context.
  - Requires no global synchronization between CPUs
- Future Work
  - MIRQ-V: Decrease LUT Demand by Optimized Delivery Invalidation
  - InterSloth: Support more RTOS Primitives (Mutexes, Alarms, Events)

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