Adding Custom Instructions to Tensilica DSPs
aka “The Modularity of TIE”

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Why bother tuning your DSP architecture? What do your customers care about?

- Performance Efficiency
- Power Efficiency
- Energy Efficiency
Introduction / Agenda

• We explore how to make TIE operations re-usable on different DSPs
  – writing in a modular, parameterisable manner
  – Varying SIMD width, operand sources, programming model (types etc)

• We explore how to make ‘C’ code more portable
  – Exploit TIE intrinsics in different DSP environments
  – Use the HAL layer to make code less “configuration dependent” and more portable

• Finally, we compare performance of simple TIE instructions across different architectures
  – SIMD width
  – Memory width
  – Memory bandwidth
Tensilica - Full Development Automation
Generates RTL + SW Development Tools

Base Processor
Example controller templates

Pre-verified Options
Off-the-shelf DSPs, Interfaces, Peripherals, Debug, etc.

Application Based
Choose a processor template

Optional Customization
With pre-verified options and/or create your own

Tensilica
Processor Generator

Processor with all customizations

Complete Hardware Design
Pre-verified RTL
EDA scripts
Test suite

Use standard ASIC/COT design techniques and libraries for any IC fabrication process

Advanced Software Tools
IDE
C/C++ compiler
Debuggers
Simulators
RTOSes

Iterate in Minutes!
The Tensilica Solution
Fully Automated Hardware and Software Tools Generation

Xtensa Processor Generator

- Custom Instructions (optional)
- Set configuration options (optional)
- Choose processor template

Xtensa Processor Generator Outputs

Hardware
- EDA scripts
- RTL

System Modeling / Design
- Instruction Set Simulator (ISS)
- Fast Function Simulator (TurboXim)
- XTSC SystemC System Modeling
- XTMP C-based System Modeling
- Pin Level co-simulation

Software Tools
- Xplorer IDE
- Graphical User Interface to all tools
- GNU Software Toolkit (Assembler, Linker, Debugger, Profiler)
- Xtensa C/C++ (XCC) Compiler
- C Software Libraries
- Operating Systems

Application Source C/C++

- Compile
- Executable
- Profile using ISS
- Optimize configuration - or - Develop custom instructions

System Development

To Fab / FPGA

Software Development

Operating Systems
Example – Population Count (aka Hamming weight)
Counting the ‘1’s in a given field

• Let’s take a simple example – “POP_COUNT_16”
  – Count the ‘1’s in 16bit fields and return an answer for each field
  – If the DSP this is attached to has a wide vector register file, we can take advantage and make a SIMD instruction and compute several (many) results per cycle

• Let’s consider two different Fusion DSPs
  – Fusion F1 – a machine with 64b registers
  – Fusion G3 – a machine with 128b registers
  – Vision P6 – a machine with 512b registers (Bonus example)
  – BBE16EP – second bonus example running in FPGA part of the demo

• How to parameterise the code to make it “work” in all situations with minimal effort?
Conceptual dataflow
We consider here the problem of 16b pop counts

Dataflow in Fusion F1
- Regfile AE_DR 64b
- Pop Count16 SIMD=4
- input 4x16b
- output 4x16b

Dataflow in Fusion G3
- Regfile vec 128b
- Pop Count16 SIMD=8
- input 8x16b
- output 8x16b
Considerations

- HW side – the register file operands that we will compute (names etc)

- HW side – the width of the register file operands and therefore the potential SIMD factor of a given implementation
  - MAX SIMD == MAX potential throughput

- SW side – what vector ctypes will we use?
  - These need to be defined in “protos”

- SW side – in our ‘C’ code we need to provide an indirection mechanism for the vector types
  - use a generic vector type in the ‘C’ and “typedef” it to suit the particular DSP we are using
Writing parameterisable TIE
Using the PERL pre-processor
What is TIE?

• TIE is a technology that is used to extend a Tensilica processor
  – Used to describe custom execution units, register files, I/O interfaces, load/store instructions, and multi-issue (FLIX) instructions
  – Includes
    – TIE language and TIE compiler
    – Software tools such as the C/C++ compiler, debugger, and instruction set simulator
    – Hardware (RTL) and implementation flows for ASIC/FPGA design

• The TIE Language is used to describe instruction extensions at a high level of abstraction
  – Syntax is a mixture of Verilog and C
  – Describes combinational relation between input and output operands
    – No need to worry about pipelining, control/bypass logic, and interfacing to other processor modules
  – Describes how the instruction extensions are used by software
Parameterising in TIE
Using the PERL pre-processor (simple usage)

```perl
#!/usr/bin/perl

my $DspType = "F1";

if("$DspType" eq "F1") {
    $RegType = "AE_DR";
    $Type64b = "ae_int64";
    $Type8xN = "ae_int64";
    $Type16xN = "ae_int16x4";
    $Type32xN = "ae_int32x2";
    $RFW = 64;
} elsif("$DspType" eq "G3") {
    $RegType = "vec";
    $Type64b = "xb_vec4Mx8";
    $Type8xN = "xb_vec4Mx8";
    $Type16xN = "xb_vec2Mx16";
    $Type32xN = "xb_vecMx32";
    $RFW = 128;
}
```

Here we define some basic variables that hold some architecture and software parameters.

- All lines starting with ";" are treated directly as PERL lines.
- In this example we need to set one variable manually – "$DspType"
- Is there a way to automate that?
  - Hint: Later ....
Parameterising in TIE
Using the PERL pre-processor (simple usage)

```verilog
/*** Function to calculate pop_count in 8 bits */
function [3:0] fn_popcount8([7:0] a)
{
    wire[3:0] address = TIEaddn(a[7], a[6], a[5], a[4],
                                a[3], a[2], a[1], a[0]);
    assign fn_popcount8 = address;
}

/*************************************************************************/
* Function to calculate pop_count in 16 bits
*************************************************************************/
function [4:0] fn_popcount16([15:0] a)
{
    wire[3:0] address0 = fn_popcount8(a[7:0]);
    wire[3:0] address1 = fn_popcount8(a[15:8]);
    assign fn_popcount16 = TIEadd(address0, address1, 1'b0);
}
```

- Some simple “building block” functions help make things more readable, and more modular.
- TIE functions are similar to Verilog “modules” – they do not create any hardware UNTIL they are instantiated somewhere.
Parameterising in TIE
Using the PERL pre-processor (simple usage)

```perl
-operation POP_COUNT_16 {out `$RegType` res, in `$RegType` src}
{
  for($i=0; $i<$RFW/16; $i++) {
    wire[15:0] w16_`$i`, res16_`$i`;
  }
  for($i=($RFW/16-1); $i>0; $i--){
    w16_`$i`;
  }
  w16_0 = src;
  for($i=0; $i<$RFW/16; $i++) {
    assign res16_`$i` = fn_zpad_5_16(fn_popcount16(w16_`$i`));
  }
  assign res = {
    for($i=($RFW/16-1); $i>0; $i--){
      res16_`$i`;
    }
    res16_0;
  }
```

- Here we can use the variables defined before to create different implementations depending on the DSP we are attaching this TIE to.

- Use of backticks "\"" forces evaluation of the variable

- Now we can see that the TIE functions really help to make the code more modular

- We instantiate one “popcount” HW per SIMD lane
Parameterising in TIE – implementation in F1
Using the PERL pre-processor (simple usage)

/***************************************************************************/
/*
* This operation performs popcounts across 16bit fields
*
***************************************************************************/
operation POP_COUNT_16 {out AE_DR res, in AE_DR src}
{
    wire[15:0] w16_0, res16_0;
    wire[15:0] w16_1, res16_1;
    wire[15:0] w16_2, res16_2;
    wire[15:0] w16_3, res16_3;
    assign {
        w16_3,
        w16_2,
        w16_1,
        w16_0} = src;
    assign res16_0 = fn_zpad_5_16(fn_popcount16(w16_0));
    assign res16_1 = fn_zpad_5_16(fn_popcount16(w16_1));
    assign res16_2 = fn_zpad_5_16(fn_popcount16(w16_2));
    assign res16_3 = fn_zpad_5_16(fn_popcount16(w16_3));

    assign res = {
        res16_3,
        res16_2,
        res16_1,
        res16_0};
}

• Here is the TIE code after the pre-processor has run
• In this case we were compiling the TIE onto “Fusion F1”
• Note the creation of 4 way SIMD engine
• Note the use of AE_DR as the source and destination registers
Parameterising in TIE – implementation in G3
Using the PERL pre-processor (simple usage)

/* This operation performs popcounts across 16bit fields */
operation POP_COUNT_16 {out vec res, in vec src}
{
    wire[15:0] w16_0, res16_0 ;
    wire[15:0] w16_1, res16_1 ;
    wire[15:0] w16_2, res16_2 ;
    wire[15:0] w16_3, res16_3 ;
    wire[15:0] w16_4, res16_4 ;
    wire[15:0] w16_5, res16_5 ;
    wire[15:0] w16_6, res16_6 ;
    wire[15:0] w16_7, res16_7 ;
    assign { w16_7, w16_6, w16_5, w16_4, w16_3, w16_2, w16_1, w16_0 } = src ;
    assign res16_0 = fn_zpad_5_16(fn_popcount16(w16_0)) ;
    assign res16_1 = fn_zpad_5_16(fn_popcount16(w16_1)) ;
    assign res16_2 = fn_zpad_5_16(fn_popcount16(w16_2)) ;
    assign res16_3 = fn_zpad_5_16(fn_popcount16(w16_3)) ;
    assign res16_4 = fn_zpad_5_16(fn_popcount16(w16_4)) ;
    assign res16_5 = fn_zpad_5_16(fn_popcount16(w16_5)) ;
    assign res16_6 = fn_zpad_5_16(fn_popcount16(w16_6)) ;
    assign res16_7 = fn_zpad_5_16(fn_popcount16(w16_7)) ;
    assign res = { res16_7, res16_6, res16_5, res16_4, res16_3, res16_2, res16_1, res16_0 } ;
}

• Here is the TIE code after the pre-processor has run
  • In this case some manual re-formatting has been done to fit the display page

• In this case we were compiling the TIE onto “Fusion G3”

• Note the creation of 8 way SIMD engine

• Note the use of vec as the source and destination registers
Parameterising in TIE – the software interface
protos – linking the world of software to the processor architecture

```
proto POP_COUNT_16 {out `$Type16xN` z, in `$Type16xN` x} {}
{
    POP_COUNT_16 z, x;
}
...

in Fusion F1 becomes

proto POP_COUNT_16 {out ae_int16x4 z, in ae_int16x4 x} {}
{
    POP_COUNT_16 z, x;
}
...

in Fusion G3 becomes

proto POP_COUNT_16 {out xb_vec2Mx16 z, in xb_vec2Mx16 x} {}
{
    POP_COUNT_16 z, x;
}
```

- protos provide the interface for the compiler to select the correct variable to pass to the intrinsic
- The Intrinsic name is the same but in F1 it's a 4-way SIMD and in G3 it's an 8-way SIMD
- protos are also used for many other software related tasks
Writing portable ‘C’ code –
Using the HAL
The Xtensa HAL – the Hardware Abstraction Layer

• A set of compile-time constants, and runtime used to abstract the details of the HW from the calling application

• In this particular case, we want to control
  – The ‘C’ types that are used to pass information to the intrinsics
  – The SIMD factor and memory accesses

• We can set all this automatically in a header file using the HAL

• Same code will therefore compile on different machines

• This is a simple example, used to show the principles
Using the HAL to define constants and types

```c
#ifndef _POPC_DEFS_H_
#define _POPC_DEFS_H_
#if XCHAL_HAVE_FUSION == 1 // really Fusion F1
#include <xtensa/tie/xt_fusion.h>
#define SIMD8 8
#define SIMD16 4
#define SIMD32 2
typedef ae_int64 vec8T;
typedef ae_int16x4 vec16T;
typedef ae_int32x2 vec32T;
#elif XCHAL_HAVE_FUSIONG3 == 1
#include <xtensa/tie/xt_pdx4.h>
#define SIMD8 16
#define SIMD16 8
#define SIMD32 4
typedef xb_vec4Mx8 vec8T;
typedef xb_vec2Mx16 vec16T;
typedef xb_vecMx32 vec32T;
#elif XCHAL_HAVE_VISION == 1
#include <xtensa/tie/xt_ivpn.h>
#define SIMD8 64
#define SIMD16 32
#define SIMD32 16
typedef xb_vec2Nx8 vec8T;
typedef xb_vecNx16 vec16T;
typedef xb_vecN_2x32 vec32T;
#endif
#endif //_POPC_DEFS_H_
```

- **XCHAL constants** are part of the HAL
- Generated with every core
- There are many of them to cover most features of the core
- Key component of writing portable software (e.g. for RTOS porting)
- Also significant runtime functions
Portable code that will run on multiple platforms

```c
/******************************************************************************
* Accelerated functions using the new TIE instructions for popcount
* **************************************************************************/

void popcount16_TIE(uint16_t * __restrict rPtr, uint16_t *data, int count)
{
    int i ;
    vec16T *vecPtr = (vec16T *) data ;
    vec16T *vecrPtr = (vec16T *) rPtr ;
    for(i=0; i<count/SIMD16; i++)
    {
        vecrPtr[i] = POP_COUNT_16(vecPtr[i]) ;
    }
}
```

- vec16T has different lengths dependent on the machine
- POP_COUNT_16 intrinsic has different SIMD width dependent on the machine
- SIMD16 #define set according to the underlying DSP width
- Code compiles unmodified on multiple different platforms
The inner loop on different targets ...
Using the exact same ‘C’ source in each case ...

- **Fusion F1**, single Loadstore, 2 16-bit calcs / cycle
- 2-way FLIX

- **Fusion G3**, dual Loadstore, 8 16-bit calcs / cycle
- Up to 4-way FLIX

- **Vision P6**, dual Loadstore, 32 16-bit calcs / cycle
- Up to 4-way FLIX
Exploiting the HAL in your TIE code

• One way to access HAL features inside TIE is to parse the relevant header file
  – xtensa-elf/arch/include/xtensa/config/core-isa.h

• Can parse this in your TIE code and then set variables accordingly:

```perl
use lib '/export/bigD/customers/new_cadence/code/tenDay_2017/work/perl' ;

#defines
# define XCHAL_HAVE_FUSION 0 /* Fusion*/
# define XCHAL_HAVE_FUSION_FP 0 /* Fusion FP option */
# define XCHAL_HAVE_FUSION_LOW_POWER 0 /* Fusion Low Power option */
# define XCHAL_HAVE_FUSION_AES 0 /* Fusion BLE/WiFi AES-128 CCM option */
# define XCHAL_HAVE_FUSION_CONVENC 0 /* Fusion Conv Encode option */
# define XCHAL_HAVE_FUSION_LFSR_CRC 0 /* Fusion LFSR-CRC option */
# define XCHAL_HAVE_FUSION_BTOPS 0 /* Fusion Bit Operations Support option */
# define XCHAL_HAVE_FUSION_AVS 0 /* Fusion AVS option */
# define XCHAL_HAVE_FUSION_16BIT_BASEBAND 0 /* Fusion 16-bit Baseband option */
# define XCHAL_HAVE_FUSION_VITERBI 0 /* Fusion Viterbi option */
# define XCHAL_HAVE_FUSION_SOFTDEMAP 0 /* Fusion Soft Bit Demap option */
# define XCHAL_HAVE_HIFI4 0 /* HiFi4 Audio Engine pkg */
# define XCHAL_HAVE_HIFI4_VFPU 0 /* HiFi4 Audio Engine VFPU option */
# define XCHAL_HAVE_HIFI3 0 /* HiFi3 Audio Engine pkg */
# define XCHAL_HAVE_HIFI3_VFPU 0 /* HiFi3 Audio Engine VFPU option */
# define XCHAL_HAVE_HIFI2 0 /* HiFi2 Audio Engine pkg */
# define XCHAL_HAVE_HIFI2EP 0 /* HiFi2EP */
# define XCHAL_HAVE_HIFI_MINI 0

• simple PERL script parses the core-isa.h file and populates the PERL hash %xchal_db with relevant variables

• Then we can use these variables to set $DspType that we set manually to start with
Calculating Hamming weight using the vector ISA
A more general example

```c
void popcount16_ISAv2(uint16_t * __restrict rPtr, uint16_t *data, int count)
{
    int i;
    vec16T *vecPtr = (vec16T *) data;
    vec16T *vecrPtr = (vec16T *) rPtr;
    vec16T m1 = *(vec16T *)&m1L;
    vec16T m2 = *(vec16T *)&m2L;
    vec16T m4 = *(vec16T *)&m4L;
    vec16T m8 = *(vec16T *)&m8L;
    vec16T h1 = *(vec16T *)&h01L;
    vec16T tmp1, tmp2, tmp3, tmp4, x;
    for(i=0; i<count/SIMD16; i++)
    {
        x = vecPtr[i];
        tmp1 = x - ((x >> 1) & m1);
        tmp2 = (tmp1 & m2) + ((tmp1 >> 2) & m2);
        tmp3 = (tmp2 + (tmp2 >> 4)) & m4;
        tmp4 = (tmp3 * h1) >> 8;
        vecrPtr[i] = tmp4 & m8;
    }
}
```

- This is basically scalar code, re-written substituting vector types for scalar types
- vec16T has different lengths dependent on the machine
- This code uses no intrinsics, only 'C' operators working on vector types
- Each DSP has a different mapping of 'C' operators to vector DSP instructions
Calculating Hamming weight using the ISA
Loop when compiled onto Fusion F1 – 4 way SIMD

- Loop is 11 instructions deep, observing in the ISS tells us “no stalls”
- 11 cycles to compute 4 results.
Calculating Hamming weight using the ISA
Loop when compiled onto Vision P6 – 32way SIMD

- No need to analyse in detail but we can see loop is unrolled by 2 (2 MULNX16)
- Loop is 9 instructions deep, observing in the ISS tells us “no stalls”
- 9 cycles to compute 64 results.
Results of different implementations (1024 calculations)
108mini provides “scalar control machine” performance

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<td>TIE 32b</td>
<td>Fast calculation on 32bit fields using TIE instruction and Vector ISA</td>
</tr>
</tbody>
</table>
Summary

• TIE provides a highly convenient mechanism for customising the Processor and the processor tool environment
  – Including the programming environment

• ... but sometimes it’s useful to make TIE code
  – modular
  – portable
  – automatic

• All the facilities are provided in the Xtensa toolset
  – HAL
  – TIE Preprocessor
The Magic of Protos™ (i)

• Protos are used extensively in the Xtensa tools to abstract, guide, “teach” the xcc compiler about the underlying architecture

• Example – Vision P6 does not contain 32x32 multiply instructions
  – We can emulate them with instruction sequences
  – Wouldn’t it be nice if we could hide that from the ‘C’/C++ programmer?
  – Consider this snippet (vec32T is a vector of 32bit numbers)

```c
vec32T h1 = *(vec32T *) &h01L ;
vec32T tmp1, tmp2, tmp3, tmp4 ;
vec32T x ;
for(i=0; i<count/SIMD32; i++)
{
  x = vecPtr[i] ;
  tmp1 = x - ((x >> 1) & m1);
  tmp2 = (tmp1 & m2) + ((tmp1 >> 2) & m2);
  tmp3 = (tmp2 + (tmp2 >> 4)) & m4 ;
  tmp4 = (tmp3 * h1) >> 24 ;
}
```

• The ‘*’ operator here must support vector 32x32 multiply – this is not available in a Vision P6 for example
• Protos can “teach” the compiler what to do
The Magic of Protos (ii)

• First we need to define the instruction sequence that creates the function we want
• Then we “link” that sequence to the operator for a given ‘C’ type ...

```c
proto MB_MUL32X32 {out xb_vecN_2x32v z, in xb_vecN_2x32v x, in xb_vecN_2x32v y}
{xb_vecN_2x64w tmp}
{
    IVP_MULUSN_2X16X32_0 tmp, x, y;
    IVP_MULAHN_2X16X32_1 tmp, x, y;
    IVP_PACKLN_2X96 z, tmp;
}
operator "*" MB_MUL32X32
```

• The “proto” statement declares a new intrinsic that takes certain ‘C’ types (already defined) and outputs an operation sequence

• The “operator” statement merely links the proto to a particular ‘C’ operator

• Note the compiler *may* optimise any of the code in the proto in the context of a loop (e.g. register MOVEs the most common candidate)
The Magic of Protos (iii)

- For a bit of fun .... we can create a new ‘C’ type “Hamming Weight Integer” and overload the “-” operator so we can calculate a hamming distance .. using no intrinsics, just ‘C’ operators.

- These two functions are essentially THE SAME (we consider the 16b case here)
The Magic of Protos (iv)

• We declare a new ctype “hw_vec16T” (Hamming Weight Vector of 16b)
  – Only SW constructs, no hardware ... just some protos ...
  – This includes some type conversions

• We declare the operation sequence to perform a Hamming Weight Difference

• We associate with the “-” operator ... then we are done 😊

• The type conversions allow the compiler to convert a vec16T ↔ hw_vec16T
  – (These are register moves which get optimised away)

• Then in the hw_vec16T domain we can define “subtract” to mean
  – XOR → POP_COUNT16 ...
  – This is the loop when compiled on Vision P6 ...

```c
{ loopgtz a4, d0000cf0 <ham_dist16_TIE+0x17c>; or a8, a2, a2; or a2, a3, a3; ivp_xor2nx8 v1, v1, v12 } 
{ ivp_sv2nx8_i v8, a8, -64; ivp_lv2nx8_ip v0, a2, 192; ivp_xor2nx8 v4, v3, v12; pop_count_16 v8, v7 } 
{ ivp_sv2nx8_ip v11, a8, 64; ivp_lv2nx8_i v3, a2, -128; nop; ivp_xor2nx8 v7, v6, v12 } 
{ ivp_sv2nx8_ip v2, a8, 192; ivp_lv2nx8_i v6, a2, -64; ivp_xor2nx8 v10, v9, v12; pop_count_16 v11, v10 } 
{ ivp_sv2nx8_i v5, a8, -128; ivp_lv2nx8_ip v9, a2, 64; pop_count_16 v2, v1; pop_count_16 v5, v4; ivp_xor2nx8 v1, v0, v12 } 
```