A new Computer Vision Processor Chip Design for automotive ADAS CNN applications in 22nm FDSOI based on Cadence VP6 Technology

Tensilica Day 2017
16th Feb. 2017, Leibniz University Hanover, Germany
DCT Company Profile

Dream Chip Technologies ...

- Positioned as a Fabless Microelectronic Engineering Company for medium to large SoC designs covering the whole range from Architecture, Specification, Design, Verification to GDSII
- Technologies: 130nm, 40nm, 28nm, 22nm FDX, 14/16nm FF
- 60 Employees/ 52 Engineers with 10 … 20 years SoC design experience
- Based in Hanover (HQ) and Hamburg, Germany
- Member of Silicon Saxony/ Germany
- Cadence Design Center Partner for Tensilica
Assisted Driving requires Cameras, Radar and Ultrasonic

Source: Texas Instruments
Use Case #1: Digital Mirroring
Use Case #1: Digital Mirroring - The Multiview

- Automotive multi camera systems for Bird-View, Rear-View and Panorama-View are a major part of today’s emerging technologies to make driving more safe and comfortable and to move towards autonomous vehicles.

Example Camera Setup (e.g. RearView)

N - Input Images

One Output Image

DreamChip - MultiView – MultiTechnology IP
Use Case #2: 360 deg Top View Camera
Use Case #3: Pedestrian detection via CNNs
Partitioning of Algorithms
Introduction – Image Sensor Processing Overview

- **Image Descriptions**
  - e.g. Triangle Meshes

- **Image Decisions**
  - e.g. Yes/No

**Computer Graphics**
- e.g. Keyboard

**Image Features**
- e.g. Motion Data

**Computer Vision**
- e.g. H.264

**Image Analysis**

**Image Pixel Data**
- e.g. RGB with 8-16 bits per Pixel

**Image Processing**
- e.g. MIPI

**Output**
- e.g. HDMI
Heterogeneous Cores for Image Sensor Processing

- **Image Descriptions**
  - e.g. Triangle Meshes

- **Image Features**
  - e.g. Motion Data

- **Image Pixel Data**
  - e.g. RGB with 8-16 bits per Pixel

- **Computer Graphics**
  - e.g. Keyboard

- **CPU**

- **Computer Vision**
  - e.g. H.264

- **Image Analysis**

- **Image Processing**
  - e.g. MIPI

- **GPU (VP)**

- **DSP (VP, CPU)**
  - e.g. HDMI

- **Vector DSP (VP, HW)**

- **Image Decisions**
  - e.g. Yes/No
Example: 360 deg Top View

- Tasks: Fish-Eye Lens correction, Stitching, Warping, Photometric synchronization for ADAS surround sensors
- Mapping:

Inputs: 4x FDP & I2C
HDMIin, HD-SDI

SW on IVP: Adaptive Tone Mappings

SW on IOP: Camera CTRL - AWB Sync.

System Interface: PCIe HDMIinout

Sensor Inputs
DMA
Local Memory
Dedicated Engines
SW Cores
Pixel-Plane Vector Processing
SW Cores
Object-Plane Scalar Processing

Streaming Interconnections

AXI Matrix
External Memory Interfacing
MPSoC Chip Architecture
Low Power CNN Architecture Proposal

ARM A53: Object Level

VP6: Pixel Level

Lock-Step

HEs: Pixel Level

Memory IF

I/O IF
**Vision P6 architecture**

- **VLIW & SIMD**: 5 issue slots
  - 64way 8-bit
  - 32way 16-bit
  - 16way 32-bit
- **ALU Ops**: 64 32-bit
  - 128 16-bit
  - 256 8-bit
- **Memory width**: 1024-bits
  - 2 vector load/store units
- **# of vector registers**: 32
- **SuperGather**: 32 non-contiguous locations read/written per instruction
- **Bus interface**: AXI4
- **iDMA**: no alignment restrictions, local memory to local memory transfers, …
- **Target frequency**: 800 MHz @ 28 nm
  - 1.1 GHz @ 16 nm
- **Optional**: Vector floating point, ECC
Convolutional neural networks (CNNs)
Why CNNs?

ImageNet experiments

- Human: 5.1%

[Image showing the comparison of different models and their error rates on ImageNet dataset, with ResNet showing significantly lower error rates compared to other models.]

Why CNNs?

• ADAS video applications using CNNs
  – Traffic sign recognition
  – Pedestrian detection
  – Image segmentation / Scene labeling
  – Object localization
  – Self driving cars
  – …
What is a CNN?

- Special case of a neural network – a deep learning based approach for high-quality object detection
- Neural network:
  - System of interconnected artificial “neurons” inspired by biological neural system
  - Neurons are the basic computation units of the brain connected with synapses
  - Connections have numeric weights, tuned during training process
  - Properly trained network will respond correctly when presented image or pattern to recognize
What is a CNN? – cont.

• Neural network organized in multiple layers
  – Fully connected layers

• CNNs have additional layers
  – Convolutional layers
  – Pooling / subsampling layers
  – Non-linear layers
What is a CNN? – cont.

- Convolutional layer:
  - Motivated by visual cortex
    - Contains cells responsible for detecting light in small, overlapping sub-regions of the visual field, called receptive fields
  - $k \times k \times D$ multiply-accumulates (MAC) required to create one element of one output feature
  - Convolution outputs 3-dimensional
  - Multiple convolutional layers
  - Results in a lot of MACs per image (see next slide)
AlexNet CNN

- 60M weighs
- ~800M multiply-accumulate to process one 227x227x3 image
- Trigger function ReLU: f(x)=max(0,x)
The SIP
Assembling the SOM...
System on Module

Overview
• DCT ADAS Heterogeneous Multi-Core Chip (22nm FDSOI Global Foundries)
• Board-to-board header with chip interfaces
• Expandable flash storage
• Power management and measurement
• Real Time Clock (RTC)
• Chip power supplies included

Benefits
• Reduced application-specific baseboard complexity
• Interfaces customizable to application requirements
• Expandable application flash storage
• Power consumption measurement
• Only Single 12 VDC power supply required

System-on-Module features
• Embedded 4GB LP-DDR4 2400 RAM
• 128MB ARM Cortex A53 storage
• 32MB ARM Cortex R5 storage
• Gigabit Ethernet PHY
• Power Management IC
• Real Time Clock (RTC)

Interfaces
• Four 300MB/s video input interfaces
• One 300MB/s video output interface
• Gigabit Ethernet
• Dual Quad-SPI for application storage
• UART, I2C, SPI, and GPIO

Dimensions
• 194mm x 100mm
4xHDMI Application Board

Overview
- DCT ADAS Quad-HDMI Base Board
- Four HDMI 1.4b inputs
- One HDMI 1.4 output
- Custom high-speed headers available
- Remote power management
- Periodic power measurement
- Gigabit Ethernet
- CAN 2.0B
- USB UART
- Video Genlock generation

Benefits
- Official reference design
- Prepared for custom sensor interfaces
- Remote system control

Base board features
- Four ADV7611 HDMI 1.4b receivers
- One ADV7511 HDMI 1.4 transmitter
- Video data rates up to 1080p60
- Two Intel MAX10 10M08DC FPGAs
- Four high-speed interface headers
- MCP2515 CAN 2.0B controller
- Gigabit Ethernet jack for SoM
- Micro-USB UART to SoM
- Micro-USB to System Controller
- Video Genlock generation
- Video input synchronization
- True output genlock possible

Dimensions
- 200mm x 180mm
Software Development Kit

Overview
- DCT ADAS Software Development Kit
- LEDE distribution with stable Linux 4.4.42
- 32-bit and 64-bit flavors available
- Tensilica LX7-VP6 development support
- Kernel API drivers

Benefits
- Official Software Development Kit
- Kernel drivers available
- Video buffer framework
- Multi-core processing examples

SDK features
- Complete ARM build environment
- LEDE distribution (lede-project.org)
- GNU ARM gcc 5.4.0
- Linux 4.4.42
- u-boot 2017.01
- musl libc 1.1.15
- 32-bit and 64-bit flavors
- all changes against respective mainline versions
- Kernel Drivers for
- QSPI, UART, I2C, Ethernet
- video framework
- Tensilica LX7-VP6 support
- Firmware control
- Debug access
**Timeline, next steps**

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Upcoming: MWC Demo (IMS LUH)
Thank You

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