## Tensilica® Products

### Common Tools, Models, Debug, Trace

<table>
<thead>
<tr>
<th>HiFi</th>
<th>Vision</th>
<th>Fusion</th>
<th>DNA</th>
<th>ConnX</th>
<th>Controllers/Custom ISAs</th>
</tr>
</thead>
</table>
| - Audio pre- and post-processing  
- Voice trigger  
- Noise reduction, audio encode and decode | - Image and vision pre-/post-processing  
- AI at the edge  
- SLAM, SGM | - Always-on sensor processing  
- Multi-purpose  
- IoT, consumer and industrial | - Standalone AI processor  
- inference at the edge  
- CNN, RNN … | - Baseband processing  
- Radar, lidar, communications  
- 5G/4G, UE, V2X, IoT and Infrastructure | - High-performance DSPs, NPUs, CPUs  
- Application-specific data types  
- Custom ISA, special functions |

### Broad Range of Application-Specific DSPs  

- Xtensa® Processor with Automated User-Defined Customization (TIE)  
- Custom
# Tensilica® Products

## HiFi
- HiFi 5 (+ VFPU / NN)
- HiFi 4 (+ VFPU)
- HiFi 3z (+ VFPU)
- HiFi 3 (+ VFPU)
- HiFi Mini

## Vision
- Vision Q7 (+ VFPU)
- Vision Q6 (+ VFPU)
- Vision P6 (+ VFPU)
- Vision C5 (+ VFPU)

## Fusion
- Fusion G6 (+ VFPU)
- Fusion G3 (+ VFPU)
- Fusion F1

## DNA
- DNA100

## ConnX
- B20 (+ VFPU / SPX)
- B10 (+ VFPU / SPX)
- BBE64EP (+ VFPU)
- BBE32EP (+ VFPU)
- BBE16EP (+ VFPU)

## Controllers/Custom ISAs
- RISC CPU (+ FPU)
- To ~ 5 Coremarks

## Custom
- Custom CPU
- User-defined ISA

## Broad Range of Application-Specific DSPs
- Xtensa® Processor with Automated User-Defined Customization (TIE)
Automated Tool, ISS, Model, RTL, and EDA Script Generation

**Base Processor**
Dozens of templates for many common applications

**Pre-Verified Options**
Off-the-shelf DSPs, interfaces, peripherals, debug, etc.

**Optional Customization**
Create your own instructions, data types, registers, interfaces

**Tensilica® IP**
Iterate in minutes!

**Customer IP**

**Complete Hardware Design**
Pre-verified Synthesizable RTL EDA scripts Test suite...

**Advanced Software Tools**
IDE C/C++ compiler Debugger ISS simulator SystemC® models DSP code libraries
Automated Tool, ISS, Model, RTL, and EDA Script Generation

Iterate in minutes!

Tensilica® IP

Customer IP

Processor Generator

Hardware
- EDA scripts
- RTL

System Modeling / Design
- Instruction Set Simulator (ISS)
- Fast Function Simulator (TurboXim)
- XTSC SystemC System Modeling
- Pin Level co-simulation
- XTMP C-based System Modeling

Verification

Block Place & Route

Synthesis

To Fab / FPGA

System Development

Software Tools
- Xplorer IDE
- GNU Software Toolkit
- Xtensa C/C++ (XCC) Compiler
- Operating Systems

Software Development

Operating Systems

C Software Libraries

Xtensa C/C++ (XCC) Compiler

GNU Software Toolkit (Assembler, Linker, Debugger, Profiler)

Xplorer IDE Graphical User Interface to all tools

Software Development

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Software Development

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Xplorer IDE Graphical User Interface to all tools
Easy DSP Software Development with Xtensa Xplorer

- Tools “know” your Processor configuration
- Launch on ISS, SystemC, RTL, FPGA, or Silicon
- Code coverage, profiling, PC trace, multi-core support
- 3rd-party JTAG debug and real-time trace
- Familiar Eclipse-based GUI
- Extensive software DSP library & examples
- Cleanly map C/C++ to SIMD & VLIW with no assembly
- High-performance optimizing C/C++ Compiler
Benchmark and Analyze
Use Xplorer to Interactively Check Performance As You Build

Check boxes to select pre-designed options

Profile your software to see the critical loops and what operations are used most

Instantly view PPA impact as you select options

Analyze performance bottlenecks with pipeline view
Tensilica® Products - HiFi

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<thead>
<tr>
<th>HiFi</th>
<th>Vision</th>
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<td>BBE64EP (+ VFPU) RISC CPU (+ FPU) To ~ 5 Coremarks</td>
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<td>BBE32EP (+ VFPU)</td>
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<td>Fusion F1</td>
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<td></td>
<td>BBE16EP (+ VFPU)</td>
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<td>HiFi 3 (+ VFPU)</td>
<td>Vision C5 (+ VFPU)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HiFi 2/EP</td>
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<tr>
<td>HiFi Mini</td>
<td></td>
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</table>

**Common Tools, Models, Debug, Trace**

**HiFi 5**
- Vision Q7 (+ VFPU)
- Vision Q6 (+ VFPU)
- Vision P6 (+ VFPU)
- Vision C5 (+ VFPU)

**HiFi 4**
- Vision Q6 (+ VFPU)
- Vision P6 (+ VFPU)
- Vision C5 (+ VFPU)

**HiFi 3z**
- Vision Q7 (+ VFPU)
- Vision P6 (+ VFPU)
- Vision C5 (+ VFPU)

**HiFi 3**
- Vision Q7 (+ VFPU)
- Vision P6 (+ VFPU)
- Vision C5 (+ VFPU)

**HiFi 2/EP**
- Vision Q7 (+ VFPU)
- Vision P6 (+ VFPU)
- Vision C5 (+ VFPU)

**HiFi Mini**
- Vision Q7 (+ VFPU)
- Vision P6 (+ VFPU)
- Vision C5 (+ VFPU)

**Broad Range of Application-Specific DSPs**

- **HiFi**
  - HiFi 5 (+ VFPU / NN)
  - HiFi 4 (+ VFPU)
  - HiFi 3z (+ VFPU)
  - HiFi 3 (+ VFPU)
  - HiFi 2/EP
  - HiFi Mini

- **Vision**
  - Vision Q7 (+ VFPU)
  - Vision Q6 (+ VFPU)
  - Vision P6 (+ VFPU)
  - Vision C5 (+ VFPU)

- **Fusion**
  - Fusion G6 (+ VFPU)
  - Fusion G3 (+ VFPU)
  - Fusion F1

- **DNA**
  - DNA100

- **ConnX**
  - B20 (+ VFPU / SPX)
  - B10 (+ VFPU / SPX)
  - BBE64EP (+ VFPU)
  - BBE32EP (+ VFPU)
  - BBE16EP (+ VFPU)

**Controllers/Custom ISAs**

- **RISC CPU** (+ FPU) To ~ 5 Coremarks
- **Custom CPU** User-defined ISA

**Custom**

- **Xtensa® Processor with Automated User-Defined Customization (TIE)**
HiFi DSPs for Audio, Voice and Speech Applications

**#1 AUDIO DSP IP**

1

**AUDIO DSP CHOICE**

**#1**

**HiFi LICENSEES WORLDWIDE**

105+

HiFi DSP FAMILY Licensees

**HiFi DSP SHIPMENTS**

1B+

HiFi DSPs SHIPPING WORLDWIDE ANNUALLY

**AUDIO ECOSYSTEM**

130+

ECOSYSTEM PARTNERS

**DIGITAL AUDIO SOFTWARE**

300+

AUDIO SOFTWARE PACKAGES


200 250 200 150 100 50
HiFi DSPs in Key Markets

**Main Functions**
- Front end processing
- Audio/Speech codecs
- Keyword/AI Speech
- Post Processing
- 3D Audio

**HiFi Advantage**
- High Performance
- Low Power/Energy
- Software Ecosystem
- Ease of Programming
- Flexibility
### 300+ Codecs and Audio/Voice Enhancement Packages

<table>
<thead>
<tr>
<th><strong>Stereo Audio</strong></th>
<th><strong>Voice</strong></th>
<th><strong>Multi-Channel</strong></th>
<th><strong>Enhancement</strong></th>
<th><strong>Enhancement</strong></th>
<th><strong>Enhancement</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>AAC</td>
<td>G.711</td>
<td>AAC, HE-AAC (Plus)</td>
<td>Accusonus</td>
<td>dbx-tv</td>
<td>Müller-BBM</td>
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<tr>
<td>HE-AAC</td>
<td>G.722</td>
<td>WMA Pro, FLAC</td>
<td>Focus-MD, Focus-</td>
<td>Total Technology</td>
<td>m/jklang® ANC,</td>
</tr>
<tr>
<td>HE-AAC Plus</td>
<td>G.723.1</td>
<td>MPEG-H</td>
<td>DNR</td>
<td>DTS</td>
<td>ASD</td>
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<tr>
<td>MP3</td>
<td>G.726</td>
<td>Dolby</td>
<td>Alango</td>
<td>TruSurround</td>
<td>NXP Software</td>
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<tr>
<td>FLAC</td>
<td>G.729AB</td>
<td>MS10, MS11,MS12</td>
<td>VCP8, VEP</td>
<td>TruVolume</td>
<td>LifeVibes</td>
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<tr>
<td>WMA 9</td>
<td>AMR-NB</td>
<td>Dolby AC-4</td>
<td>Arkamys</td>
<td>TruDialog</td>
<td>VoiceExperience</td>
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<tr>
<td>WMA 10 Pro</td>
<td>AMR-WB</td>
<td>Dolby Atmos</td>
<td>ImmerseU</td>
<td>TruTools</td>
<td>QNX ANC</td>
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<tr>
<td>REAL Audio 8, 9, 10</td>
<td>EVS</td>
<td>Digital AC-3 and Plus</td>
<td>Sound Staging</td>
<td>TruGaming</td>
<td>QSound microQ</td>
</tr>
<tr>
<td>Ogg Vorbis</td>
<td>GSM-HR</td>
<td>DDCE, True HD</td>
<td>AM3D</td>
<td>WOW XT</td>
<td>m</td>
</tr>
<tr>
<td>AMR WB+</td>
<td>GSM-FR</td>
<td>Pro Logic II/llx</td>
<td>Diesel Power, Zirene</td>
<td>Fortemedia</td>
<td>NXP Software</td>
</tr>
<tr>
<td>SBC Bluetooth</td>
<td>GSM-EFR</td>
<td>Dolby Mobile 3+</td>
<td>Audyssey</td>
<td>iS620, iS700, iS800</td>
<td>LifeVibes</td>
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<tr>
<td>BSAC</td>
<td>AAC-ELD</td>
<td>DS1, DAa2, DAx3</td>
<td>Dynamic Volume and</td>
<td>Harman Clari-Fi</td>
<td>VoiceExperience</td>
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<tr>
<td>DAB</td>
<td>Opus</td>
<td>Dolby Digital Live</td>
<td>EQ</td>
<td>Hillcrest Labs</td>
<td>QSound microQ</td>
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<tr>
<td>DAB+</td>
<td>mSBC</td>
<td>HD Master Audio</td>
<td>Cadence</td>
<td>Freespace</td>
<td>MQFX MQvoice</td>
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<tr>
<td>DRm (xHE-AAC)</td>
<td>CVSD</td>
<td>Express</td>
<td>Sample Rate</td>
<td>Kronoton</td>
<td>Retune DSP</td>
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<tr>
<td>APE</td>
<td>Skype SILK</td>
<td>Transcoder, Neo:6</td>
<td>Converter</td>
<td>HDSX</td>
<td>Beamform, AEC</td>
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<td></td>
<td>AEC</td>
<td>Broadcast, DMP, M6</td>
<td>PDM=&gt;PCM</td>
<td>Malaspinna</td>
<td>Rubidium</td>
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<tr>
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<td>LEC</td>
<td>Neural Surround</td>
<td>Converter</td>
<td>VoiceBoost</td>
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<td>DTS Interactive</td>
<td>Conexant</td>
<td>Maxim</td>
<td>Sensory</td>
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<td>Headphone:X</td>
<td>AudioSmart</td>
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<td>Cywee</td>
<td>Management</td>
<td>Sonic Emotion</td>
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<td>MightWorks</td>
<td>Absolute 3D</td>
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<td>Call Solution+SRE</td>
<td>SPL Vitalizer</td>
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<td>Waves Audio</td>
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<td></td>
<td>MAXXAudio, Voice, Nx</td>
</tr>
</tbody>
</table>
# Tensilica® Products - Vision

<table>
<thead>
<tr>
<th>HiFi</th>
<th>Vision</th>
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<td>HiFi 5 (+VFPU/NN)</td>
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<td>B10 (+VFPU/SPX)</td>
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<tr>
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<td>BBE64EP (+VFPU)</td>
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<td>HiFi 3 (+VFPU)</td>
<td>Vision C5 (+VFPU)</td>
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<td>BBE32EP (+VFPU)</td>
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<tr>
<td>HiFi 2/EP</td>
<td></td>
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<td>BBE16EP (+VFPU)</td>
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</tr>
<tr>
<td>HiFi Mini</td>
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<td></td>
<td></td>
<td>Custom CPU User-defined ISA</td>
</tr>
</tbody>
</table>

- **HiFi 3z** (+VFPU)
- **HiFi 4** (+VFPU)
- **HiFi 5** (+VFPU/NN)
- **HiFi 2/EP**
- **HiFi Mini**

## Broad Range of Application-Specific DSPs

- HiFi 3
- HiFi 2/EP
- HiFi Mini

## Custom

- **Xtensa® Processor with Automated User-Defined Customization (TIE)**

---

- **HiFi 5** (+VFPU/NN)
- **HiFi 4** (+VFPU)
- **HiFi 3z** (+VFPU)
- **HiFi 3** (+VFPU)
- **HiFi 2/EP**
- **HiFi Mini**

- **Vision Q7** (+VFPU)
- **Vision Q6** (+VFPU)
- **Vision P6** (+VFPU)
- **Vision C5** (+VFPU)

- **Fusion G6** (+VFPU)
- **Fusion G3** (+VFPU)
- **Fusion F1**

- **DNA100**

- **ConnX**
  - **B20** (+VFPU/SPX)
  - **B10** (+VFPU/SPX)
  - **BBE64EP** (+VFPU)
  - **BBE32EP** (+VFPU)
  - **BBE16EP** (+VFPU)

- **Controllers/Custom ISAs**
  - **RISC CPU** (+FPU) To ~ 5 Coremarks
  - **Custom CPU User-defined ISA**

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Vision Recent Customer Success

- Vision P5 & P6 DSP
- Integrated in AI Processing Unit (P60)\(^1\)
- 35+ Smartphone designs\(^2\)

- Vision P5 & P6 DSP
- For 3D sensing, HMI, AR/VR apps
- 100+ Smartphone designs\(^3\)

- Hi3559AV100, Hi3519AV100 new-generation intelligent video processor
- Hi3359A (4x P6), Hi3519A (1x P6)
- High-End Surveillance, professional camera, drone camera, extreme sports motion DV

- Vision P5 DSP\(^5\)
- Creates high-resolution 3D images in real time based on advanced RF technology
- Targeted for smart home, automotive, smart retail, robotics markets

---

Source: 1, 2, 3, 4, 5

- GW5400, the World’s First Automotive Smart Viewing Camera Processor
- Vision P5
- Zero airflow environment, smart rear-view mirror, backup-camera
# Vision Product Comparison Chart

<table>
<thead>
<tr>
<th>Use Case</th>
<th>Vision P6</th>
<th>Vision Q6</th>
<th>Vision Q7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vision and Low-end AI (up to 256GMAC/sec)</td>
<td>Vision and Low-end AI (up to 384GMAC/sec)</td>
<td>Vision and Low-end AI (up to 768GMAC/sec)</td>
</tr>
<tr>
<td></td>
<td>(maximizing MHz)</td>
<td>(maximizing MHz)</td>
<td>(maximizing MHz)</td>
</tr>
<tr>
<td><strong>MACs</strong></td>
<td><strong>8x8</strong></td>
<td><strong>256</strong></td>
<td><strong>256/512</strong> (Optional)</td>
</tr>
<tr>
<td><strong>(Higher MAC = Higher Compute)</strong></td>
<td><strong>8x16</strong></td>
<td><strong>128</strong></td>
<td><strong>128</strong></td>
</tr>
<tr>
<td></td>
<td><strong>16x16</strong></td>
<td><strong>64</strong></td>
<td><strong>64/128</strong> (Optional)</td>
</tr>
<tr>
<td><strong>Vector Floating Point Unit</strong></td>
<td><strong>16b Half Precision</strong></td>
<td><strong>32 way SIMD (optional)</strong></td>
<td><strong>2X 32 way SIMD (Optional)</strong></td>
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<tr>
<td></td>
<td><strong>32b Single Precision</strong></td>
<td><strong>16 way SIMD (optional)</strong></td>
<td><strong>2x 16way SIMD (Optional)</strong></td>
</tr>
<tr>
<td><strong>MAX SIMD Width</strong></td>
<td><strong>64 way 8bit</strong></td>
<td><strong>64 way 8 bit</strong></td>
<td><strong>64 way 8 bit</strong></td>
</tr>
<tr>
<td><strong>SuperGather (Scatter Gather)</strong></td>
<td><strong>Yes</strong></td>
<td><strong>Yes</strong></td>
<td><strong>Yes</strong></td>
</tr>
</tbody>
</table>
Tensilica: Comprehensive Vision Software Solutions
Full ecosystem of software frameworks and compilers for all vision programming styles

- OpenCL
  - Halide
    - Halide Compiler
  - OpenCL Compiler (LLVM)
  - OpenCL Runtime
  - OpenCL BIFL library
  - DMA Manager (libidma)

- Embedded C/C++
  - Xtensa C/C++ Compiler (XCC & LLVM)
  - Tile Manager
  - OpenVx Runtime*

- OpenVx Graph*
  - OpenVx Toolkit*

- OpenVx/OpenCL Host Code
  - OpenVx/OpenCL Host Code

- Linux Host CPU (Xtensa or Other)

- User Code
  - Cadence Compiler / Tool
  - Cadence SW library / Runtime
  - Cadence Tensilica DSP

*Not supported on Vision Q7
Tensilica® Products – Fusion G

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<td>HiFi 3z (+ VFPU)</td>
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<td>Fusion F1</td>
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<td>BBE64EP (+ VFPU)</td>
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<tr>
<td>HiFi 3 (+ VFPU)</td>
<td>Vision C5 (+ VFPU)</td>
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<td>BBE32EP (+ VFPU)</td>
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<tr>
<td>HiFi 2/EP</td>
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<td>BBE16EP (+ VFPU)</td>
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<tr>
<td>HiFi Mini</td>
<td></td>
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</tr>
</tbody>
</table>

- Broad Range of Application-Specific DSPs
- HiFi 3/EP, HiFi 2/EP, HiFi Mini
- HiFi 3z, HiFi 4, HiFi 5
- Fusion F1, Fusion G1, Fusion G3, Fusion G6
- Vision Q5, Vision Q6, Vision Q7
- HiFi 3, HiFi 4, HiFi 5

Custom Tools, Models, Debug, Trace

- Fusion F1
- Fusion G1, Fusion G3, Fusion G6
- Vision Q5, Vision Q6, Vision Q7
- HiFi 3, HiFi 4, HiFi 5

Broad Range of Application-Specific DSPs

- Xtensa® Processor with Automated User-Defined Customization (TIE)
Trends in Multiple Markets Driving the Need for Fusion G Family

More floating-point use…
- Algorithms and codecs in floating point
- Time-to-market benefits
- Out-of-box performance
- Easy to program and optimize

Multi-purpose…
- Run multiple algorithms on one ISA
- Fixed- and floating-point DSP
- Support for multiple data types
- Efficient real-time control
Target Applications for Fusion G Family

- Noise/Echo Cancellation
- Surround Sound
- Motor Control
- Radar Processing
- Low-End Image Processing
- General Signal Processing
- Baseband Processing
- Sensor Fusion
# Tensilica® Products – DNA (AI inference)

## HiFi
- **HiFi 5** (+VFPU / NN)
- **HiFi 4** (+VFPU)
- **HiFi 3z** (+VFPU)
- **HiFi 3** (+VFPU)
- **HiFi 2/EP**
- **HiFi Mini**

## Vision
- **Vision Q7** (+VFPU)
- **Vision Q6** (+VFPU)
- **Vision P6** (+VFPU)
- **Vision C5** (+VFPU)

## Fusion
- **Fusion G6** (+VFPU)
- **Fusion G3** (+VFPU)
- **Fusion F1**

## DNA
**DNA100**

## Common Tools, Models, Debug, Trace

## ConnX
- **B20** (+VFPU / SPX)
- **B10** (+VFPU / SPX)
- **BBE64EP** (+VFPU)
- **BBE32EP** (+VFPU)
- **BBE16EP** (+VFPU)

## Controllers/Custom ISAs
- **RISC CPU** (+FPU)
- **To ~ 5 Coremarks**
- **Custom CPU**
  - User-defined ISA

## Broad Range of Application-Specific DSPs

## Custom

**Xtensa® Processor with Automated User-Defined Customization (TIE)**
### AI Inference at the Edge Processing Needs

<table>
<thead>
<tr>
<th>Scalability</th>
<th>IoT, Mobile, Surveillance, AR/VR, Automotive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>&lt;0.5TMAC to 100sTMAC</td>
</tr>
<tr>
<td>Increase in Compute Requirement</td>
<td>Higher Resolution</td>
</tr>
<tr>
<td></td>
<td>Move from Traditional to AI</td>
</tr>
<tr>
<td>Latency Critical Applications</td>
<td>AR/VR</td>
</tr>
<tr>
<td></td>
<td>Automotive</td>
</tr>
<tr>
<td>Higher Power Efficiency</td>
<td>Battery Life</td>
</tr>
<tr>
<td></td>
<td>Bandwidth Constraints</td>
</tr>
<tr>
<td>Flexibility</td>
<td>Continuously adapting/changing market needs</td>
</tr>
</tbody>
</table>
Tensilica® DNA 100 Key Features

**Scalability**
- Supports 256, 512, 1K, 2K Physical 8b MAC configurations
- Single click configuration select

**Throughput**
- Sparse compute hardware engine avoids multiply by 0 (activation & weights)
- Significant higher throughput and lower power compared to traditional dense compute engines

**Bandwidth**
- Compressor/Decompressor hardware block avoids data movement of 0 (activation & weights)
- Efficient memory management

**Programmable**
- Integrated Vision P6 provides flexibility to support any hardware unsupported layer efficiently
- Integrated Vision P6 provides extensibility through TIE

**Standalone**
- Efficient convolution & fully connected layer support through high MAC occupancy rate
- Integrated VPU supports commonly used non-convolution layers
Tensilica Neural Network Compiler

**Key Features**

- Support for DNA 100, Vision Q6, Vision C5, Vision P6 DSPs
- Support for Windows and Red Hat Linux
- Custom Layer
- Analyzer enables:
  - prioritize accuracy vs performance
  - Min/Max range control to guide quantization
- Optimizer enables:
  - Efficient memory management (ex. avoid unnecessary roundtrips, local memory partitioning and buffering)
  - Tile & DMA management
  - Graph transformation (ex. fusion, elimination)
- NN library showcasing processor specific optimized functions
# Tensilica® Products - ConnX

<table>
<thead>
<tr>
<th>HiFi</th>
<th>Vision</th>
<th>Fusion</th>
<th>DNA Standalone AI processor</th>
<th>ConnX</th>
<th>Controllers/Custom ISAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>HiFi 5 (+ VFPU / NN)</td>
<td>Vision Q7 (+ VFPU)</td>
<td>Fusion G6 (+ VFPU)</td>
<td>DNA100</td>
<td>B20 (+ VFPU / SPX)</td>
<td>RISC CPU (+ FPU) To ~ 5 Coremarks</td>
</tr>
<tr>
<td>HiFi 4 (+ VFPU)</td>
<td>Vision Q6 (+ VFPU)</td>
<td>Fusion G3 (+ VFPU)</td>
<td></td>
<td>B10 (+ VFPU / SPX)</td>
<td>Custom CPU User-defined ISA</td>
</tr>
<tr>
<td>HiFi 3z (+ VFPU)</td>
<td>Vision P6 (+ VFPU)</td>
<td>Fusion F1</td>
<td></td>
<td>BBE64EP (+ VFPU)</td>
<td></td>
</tr>
<tr>
<td>HiFi 3 (+ VFPU)</td>
<td>Vision C5 (+ VFPU)</td>
<td></td>
<td></td>
<td>BBE32EP (+ VFPU)</td>
<td></td>
</tr>
<tr>
<td>HiFi 2/EP</td>
<td></td>
<td></td>
<td></td>
<td>BBE16EP (+ VFPU)</td>
<td></td>
</tr>
<tr>
<td>HiFi Mini</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Broad Range of Application-Specific DSPs

- **HiFi**
  - HiFi 5 (+ VFPU / NN)
  - HiFi 4 (+ VFPU)
  - HiFi 3z (+ VFPU)
  - HiFi 3 (+ VFPU)
  - HiFi 2/EP
  - HiFi Mini

- **Vision**
  - Vision Q7 (+ VFPU)
  - Vision Q6 (+ VFPU)
  - Vision P6 (+ VFPU)
  - Vision C5 (+ VFPU)

- **Fusion**
  - Fusion G6 (+ VFPU)
  - Fusion G3 (+ VFPU)
  - Fusion F1

- **DNA Standalone AI processor**
  - DNA100

- **ConnX**
  - B20 (+ VFPU / SPX)
  - B10 (+ VFPU / SPX)
  - BBE64EP (+ VFPU)
  - BBE32EP (+ VFPU)
  - BBE16EP (+ VFPU)

## Custom

- **DNA**
  - BBE16EP
  - BBE32EP
  - BBE64EP
  - B20
  - B10

- **Fusion**
  - Fusion G6
  - Fusion G3
  - Fusion F1

- **DNA Standalone AI processor**
  - DNA100

## Xtensa® Processor with Automated User-Defined Customization (TIE)
• Radar / Comms / OFDM domain-optimized DSP with rich feature set
  – Optimal for many classes of algorithm
    – FFT, filters, matrix operations, math functions
  – Native support for complex and real datatypes
    – In fixed point or optional vector floating point

• Scalable solution – 5 family members BBE16/32/64EP & B10/20
  – A family of DSPs with source code compatibility
    – Wide choice of PPA points for multiple applications with same source and tools
  – The same ISA is implemented in SIMD8, SIMD16 or SIMD32
    – 16-bit real and complex values (datapath is 128b, 256b, 512b)
    – 32-bit real and complex values on B10/20 (datapath is 256b, 512b)

• Datapath-width-tuned SIMD & VLIW architecture + local memory access
  – L1 access is 128b, 256b, 512b
  – Two L1 memory accesses per cycle allowed – up to 1024b / cycle
  – Optional integrated DMA engine has its own AXI4 master port
    – With access to L1 memories and can run “in the background”

Automated User-Defined Customization

Xtensa® Processor Generator
Highlights of ConnX DSP enhanced performance
BBE16/32/64EP and B10/20

Optimal DSP engines
• Highly efficient MAC/ALU usage with broad DSP ISA

Broad range of DSPs buildable from a single platform
• Code compatible for ease of portability for performance scalability
• Scale to meet your needs: 16, 32, 64 and 128 MACs…
• Easily select useful options with click boxes
• Software tools and verification is automatic

Optimized for low power/energy
• Clock and data gating implemented, plus logic and memory bus gating are also options
• Loop buffer can reduce instruction memory accesses
• ISA acceleration reduces cycle counts

Limited area and power increase as frequency is increased
Libraries for ConnX DSPs

Rich and optimized DSP libraries for basic and advanced DSP functions
– Vector fixed/floating-point, real/complex support
– Library source code available

*Note: To cover the complete library routine list, all optional configurations have to be selected*

<table>
<thead>
<tr>
<th>Category</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Math</td>
<td>Scalar and vector for: arc cosine/sine/tangent, cosine/sine/tangent/cotangent, hyperbolic sine/cosine/tangent, sigmoid, logarithm, anti-logarithm, exponential, square root, reciprocal, reciprocal square root</td>
</tr>
<tr>
<td>Complex</td>
<td>Magnitude, phase, conjugate, exponent, combined cosine and sine, normalization, division, polar to cartesian and cartesian to polar conversion</td>
</tr>
<tr>
<td>FIR Filters</td>
<td>Convolution, auto/cross correlation, interpolation, decimation, polynomial fitting/interpolation</td>
</tr>
<tr>
<td>IIR Filters</td>
<td>Biquad, lattice block IIR</td>
</tr>
<tr>
<td>FFT</td>
<td>Complex, real, FFT/IFFT, DFT</td>
</tr>
<tr>
<td>Vector</td>
<td>Product, sum, magnitude, reciprocal, division, transcendental, peak, mean</td>
</tr>
<tr>
<td>Matrix</td>
<td>Multiply, transpose/Hermitian, Cholesky/QR decomposition and recursion, determinant, inverse, linear equation solution</td>
</tr>
<tr>
<td>Communication Systems</td>
<td>CRC, de-spreading, modulation, slicer, convolutional encoding, bit manipulation, PRBS Generation, space time coding</td>
</tr>
</tbody>
</table>
### Tensilica® Products – Controllers and Customisation

#### Broad Range of Application-Specific DSPs

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<td></td>
<td>B10 (+VFPU/SPX)</td>
<td></td>
</tr>
<tr>
<td>HiFi 3z (+VFPU)</td>
<td>Vision P6 (+VFPU)</td>
<td>Fusion F1</td>
<td></td>
<td>BBE64EP (+VFPU)</td>
<td>Custom CPU User-defined ISA</td>
</tr>
<tr>
<td>HiFi 3 (+VFPU)</td>
<td>Vision C5 (+VFPU)</td>
<td></td>
<td></td>
<td>BBE32EP (+VFPU)</td>
<td></td>
</tr>
<tr>
<td>HiFi 2/EP</td>
<td></td>
<td></td>
<td></td>
<td>BBE16EP (+VFPU)</td>
<td></td>
</tr>
<tr>
<td>HiFi Mini</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### HiFi 3

- HiFi 5 (+VFPU/NN)
- HiFi 4 (+VFPU)
- HiFi 3z (+VFPU)
- HiFi 3 (+VFPU)
- HiFi 2/EP
- HiFi Mini

#### Fusion

- Fusion G6 (+VFPU)
- Fusion G3 (+VFPU)
- Fusion F1

#### DNA Standalone AI processor

- DNA100

#### ConnX

- B20 (+VFPU/SPX)
- B10 (+VFPU/SPX)
- BBE64EP (+VFPU)
- BBE32EP (+VFPU)
- BBE16EP (+VFPU)

#### Custom

- Custom CPU User-defined ISA

---

**Xtensa® Processor with Automated User-Defined Customization (TIE)**

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Base RISC Capabilities

• Xtensa defines Powerful RISC ISA

• Available in LX or NX pipelines
  – Trade clock speed vs extreme flexibility

• Can be used for tiny control tasks

• Can be used for high performance general processing

• Good debug, trace features
Configurability – features and performance

• High degree of configurability
  – Base RISC ISA – tune to likely requirements (MUL, DIV, interrupt, debug, trace ..)
  – Supports optional single and double precision Floating point
  – Caches or TCM

• Can have user-defined extensions through TIE language
  – Could be new calculation operations
  – Register files, addressing modes
  – Interfaces to HW engines

• Up to 5 Coremarks
  – High performance multi-issue controllers
Differentiate with a custom ISA using “TIE”, automatic tools support

**Tensilica Instructions Extensions**

- Simple Verilog-like language, where you can define...
  - Input/output queues and ports
  - Custom register files
  - Fast lookup tables and local memories
  - Simple single-cycle or multi-cycle instructions
  - SIMD for vectorization
  - FLIX (VLIW) for grouping parallel operations into one instruction

---

**Example: Popcount acceleration**

Create a `pop_count` instruction that counts the one’s in a 32-bit register by adding the bits together. This simple Verilog-like code is all it takes to create both the pre-verified adder RTL (175 gates) and the instruction:

```
operation pop_count { out AR co, in AR ci}{}
    wire [5:0] sum = a0 + a1 + a2 + a3;
    assign co = {26'b0, sum};
```

Best hand-coded ASM using standard instructions takes >10 cycles. This simple instruction takes it down to just one cycle for 10x speedup.
Vision Q7
Tensilica Vision Q7 DSP: 6th-Generation Vision and AI DSP

Follow on to the Vision Q6 DSP for Vision and AI:
Achieves 1.7GHz**/1.55** GHz peak frequency

- Up to 1.7X higher TOPS in the same area
  Delivers up to 2.06** TOPS/ 1.82* TOPS

- Up to 2X performance for vision/AI applications, including floating-point performance

- Up to 2X GMAC/mm² and GFLOPS/mm²

• * 16nm process with OD
• ** 1.7GHz in 7nm with OD
• ® Vision Q7 DSP performance is relative to the Vision Q6 DSP
Software Ecosystem
Tensilica: Comprehensive Vision Software Solutions
Full ecosystem of software frameworks and compilers for all vision programming styles

- **OpenCL**
- **Halide**
- **Embedded C/C++**
- **OpenVx Graph***

**Halide Compiler**

- **OpenCL Compiler (LLVM)**
- **OpenCL Runtime**
- **OpenCL BIFL library**
- **DMA Manager (libidma)**
- **XTOS (Single Thread) or XOS (Multithread) or Commercial RTOS**

**OpenVx Toolkit***

- **Xtensa C/C++ Compiler (XCC & LLVM)**
- **Tile Manager**
- **OpenVx Runtime***
- **OpenCV based Imaging Library (lib “XI”)**
- **OpenVx/OpenCL Host Code**

**Vision P6 / Q6 / Q7 DSP**

**Linux Host CPU (Xtensa or Other)**

*Not supported on Vision Q7
XI-Library: Accelerates Commonly used OpenCV functionality

**XI-Library**
- Tile based processing for chaining of functions in local memory to efficiently use memory bandwidth
- Specific kernel sizes, data types and modes as part of API to avoid excessive checking inside the function for every tile
- Uses more efficient data structures for images and tiles instead of OpenCV structures that waste local memory
- In most cases, function works on image planes to avoid frequent deinterleaving of interleaved image data

**XI Library Deliverables**
- XI Library source code workspace: Delivered with XPG
- XI Library performance
- XI Library user’s guide

**XI-Library Example Functions**
- Image Proc Modules: Convolution functions, Geometric Functions,…
- Features Modules: Feature Detection, Feature Descriptor
- Motion Analysis & background analysis
- Core modules: Binary elements, bitwise operation, vector operations…
## Detail Description of XI Library Functions (few examples)

<table>
<thead>
<tr>
<th>XI Library Module</th>
<th>Sub Module</th>
<th>Example functions (subset)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Image Proc module</strong></td>
<td>Convolution functions</td>
<td>xIBilaterfilter, xBoxfilter, xICannyedge</td>
<td>“Image processing” module contains functions related to geometrical image transformations, scaling, 2D convolution, edge detection</td>
</tr>
<tr>
<td></td>
<td>Geometric transformation</td>
<td>xIResizeBilinear, xITranspose, xIWarpAffine</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Structural analysis</td>
<td>xIConnectedComponents</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Miscellaneous transforms</td>
<td>xICvtColor, xIntegral, xIntegralSqr</td>
<td></td>
</tr>
<tr>
<td><strong>Features module</strong></td>
<td>Feature detection</td>
<td>xICornerHarris, xIFAST</td>
<td>Feature detection and description functions contained in the “features2D” module</td>
</tr>
<tr>
<td></td>
<td>Feature descriptor</td>
<td>xIBRIEF</td>
<td></td>
</tr>
<tr>
<td><strong>Video/Motion Analysis module</strong></td>
<td>Motion analysis</td>
<td>xIAccumulateWeighted, xIMeanShift, xIOpticalFlow_TrackPoint</td>
<td>“Video” module contains functions related to video processing.</td>
</tr>
<tr>
<td></td>
<td>Background subtraction</td>
<td>xIBS_MOG</td>
<td></td>
</tr>
<tr>
<td><strong>Core module</strong></td>
<td>Utility functions</td>
<td>xIErrStr, xICopytile, xIFillTile</td>
<td>“Core” module includes low-level support and helper functions</td>
</tr>
<tr>
<td></td>
<td>Unary element wise operations</td>
<td>xIAbs, xIBitwiseNot, xIClip, …</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Binary element wise operations</td>
<td>xIAbsdiffScalar, xIAddScalar, xIBitwiseAndScalar, …</td>
<td></td>
</tr>
<tr>
<td></td>
<td>with scalar value</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Binary element wise operations</td>
<td>xIAbsdiff, xIAdd, xIBitwiseOr, …</td>
<td></td>
</tr>
<tr>
<td></td>
<td>with scalar value</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reduction operations</td>
<td>xICountNonZero, xIGatherLocationsEQ, xIMaxLoc, …</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vector operations</td>
<td>xIMagnitude, xIPhase, xIPolarToCart, …</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Miscellaneous operations</td>
<td>xIExtractChannel, xILUT, xIMerge2/xIMerge3, …</td>
<td></td>
</tr>
</tbody>
</table>
Example of Lane Departure Warning: Work done at Cadence

Use of XI-Lib
Android Neural Network (ANN) API
Support for Android 8.1 Oreo ANN release

**Host**
- Graph Executor decides to
  - execute graph/sub-graph/layer
  - Selects full layer kernel
  - Tile & DMA management*
  - Data/weight rearrangement
- XRP sends commands to DSP

**DSP**
- NN HAL Command Interpreter
  - Interprets commands from XRP to full layer kernel
- Full layer kernel
  - Allocates local memory
  - Loops over tiles, DMAs data, invokes library
- XI CNN Library
  - Optimized library using Google’s Quantization scheme

* Not needed with Vision DSP

## Vision and AI Software Status: Vision Q7

<table>
<thead>
<tr>
<th>SW Pkg</th>
<th>Current Release</th>
<th>Next Release/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example SW package is available today with XPG Released with RI.1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Various SW Kernels</th>
<th>Current Release</th>
<th>Next Release/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>All SW kernel listed in P6 vs Q7 comparison are available today (17,18,19). They are all optimized for Vision Q7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>XI-Lib</th>
<th>Current Release</th>
<th>Next Release/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>First release: Released 8.0.1 released with RI.1 Available with XPG</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>XNNC</th>
<th>Current Release</th>
<th>Next Release/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>XNNC 1.5 for baseline 256 MAC available now</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ANN</th>
<th>Current Release</th>
<th>Next Release/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline 256 MAC for Android Q: to be release by end of August 2019 Planning to align with Android Q release After we release Vision P6 for Android Q by end of August 2019</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OpenCL</th>
<th>Current Release</th>
<th>Next Release/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Available now Released with 2019.1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Halide</th>
<th>Current Release</th>
<th>Next Release/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>End of Aug 2019</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>