Novel FPGA-Architecture
Technical Features FPGA
(Field Programmable Gate Array)

• Configurable digital circuit
• Function is not defined during the manufacturing process, but through configuration.
• Unlike a microprocessor, not program-controlled
• Any logical (boolean) functions can be configured
• Circuit elements are connected by configurable routing connections
• Very fast, as non clocked circuits can be realized as well
• Fast Time to Market
• More difficult to copy than conventional circuits
• Changes to existing hardware possible by loading new configuration
• Realizes function of an ASIC (Application Specific Integrated Circuit) without Mask costs and additional production time
Novel architecture of the Cologne Chip FPGA

- Double checkerboard architecture:
  There are only switch boxes on every second field
  Big and small switchboxes alternate

- Extremely small LUTs (Look UpTable)

- Complex Configurable Element (CPE) with the following properties:
  8 combinatorial inputs with 7 LUT2
  2 flip-flops or latches
  2 routed outputs, 2 outputs for additional functions
  2 cascaded, not routed connections in the X and Y directions
  very flexible clock routing, plus 4 global clocks
  CPE can be configured with 2x 4 inputs or 1x 8 inputs
  CPE can be 2-bit full-adder or 2x2 multiplier

- Configuration memory of 8-bit latches leads to low internal routing and
  low SEU probability.

- 12 routing layers simplifies Place & Route software.

- Direction Change Multiplexer allows direction change of a signal in
  every switchbox
Commercial Situation in the FPGA world market

- 2 large and 2 smaller companies
- All US-based
- Almost all analysts expect the market to continue to grow strongly.

Companies (revenue and EBIT 2018 in million $US in the FPGA segment):

- XILINX: Sales: 2,540, EBIT: 750
- Intel PSG (formerly Altera): Sales: 2,100, EBIT: 500
- Lattice: Sales: 200, EBIT: -50 (estimated)

- So the world market is about $US 5 billion.
- With the exception of Lattice, all FPGA manufacturers earn approx. 30% EBIT.
- Even with market shares in the lower single-digit percentage range, Cologne Chip has very attractive commercial opportunities. There are also special Market entry advantages as the only manufacturer in Europe and also "Made in Europe".
Central Programmable Element (CPE)

Signals of a CPE (fixed connections in green, RAM-connections in blue)
I/O Block as Interface to chip outside

Simplified circuit diagram of I/O block
Switchbox (small) for Routing
Switchbox (big) for Routing
Switchbox-Routing in one dimension

Channel width 7

Long range signal bus

Long range buffer
Interconnections of CPEs with Switchboxes
Interconnections of FPGA Circuit Elements

Only Output CPEs
Overview: Strukture of the FPGA
Overall View of the FPGA Die
Package of the FPGA: 320 ball LFBGA
### Package Connections of the FPGA
(ball positions and Signal names)

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| A | GND | SER_RX_N | SER_TX_N | GND | IO_N1_A2 | IO_N1_A3 | VDD_N1 | IO_N1_A5 | IO_N1_A6 | IO_N2_A7 | IO_N2_A5 | GND | IO_N2_A7 | IO_E2_E8 | IO_E2_E7 | VDD_N2 | IO_E2_E8 | VDD_N2 | IO_E2_E7 |
| B | SER_TX_P | SER_RX_P | PORT_ADJ | IO_N0_A0 | IO_N0_A2 | IO_N0_A3 | GND | IO_N0_A6 | IO_N0_A7 | IO_N0_A6 | VDD_N0 | GND | VDD_N0 | IO_E2_A6 | GND | VDD_N0 | GND | VDD_N0 | GND |
| C | VDD | VDD | SER_TX | IO_N1_A0 | IO_N1_A1 | IO_N1_A2 | GND | IO_N1_A4 | IO_N1_A5 | IO_N1_A4 | GND | IO_N1_A4 | VDD_N1 | VDD | VDD | GND | VDD | VDD | VDD |
| D | GND | CLK | TST | RST_N | IO_N1_A1 | IO_N1_A2 | GND | IO_N1_A4 | IO_N1_A5 | IO_N1_A4 | GND | IO_N1_A4 | VDD_N1 | GND | GND | GND | GND | GND | GND |
| E | CLKB | GND | GND | GND | GND | GND | VDD | GND | GND | GND | GND | VDD | GND | GND | GND | GND | VDD | GND | GND |
| F | IO_W2 | IO_W2 | IO_W2 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| G | IO_W2 | IO_W2 | IO_W2 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| H | GND | VDD | W2 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | VDD | GND | GND |
| J | IO_W1 | IO_W1 | IO_W1 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| K | IO_W0 | IO_W0 | IO_W0 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| L | IO_W0 | IO_W0 | IO_W0 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| M | IO_W0 | IO_W0 | IO_W0 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| N | GND | VDD | W2 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| P | IO_W1 | IO_W1 | IO_W1 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| R | IO_W1 | IO_W1 | IO_W1 | GND | GND | GND | VDD | GND | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| T | CFG_MD0 | CFG_MD1 | CFG_MD2 | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| U | CFG_MD2 | CFG_MD1 | CFG_MD0 | VDD | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND |
| V | GND | CFG_MD0 | CFG_MD1 | GND | VDD | GND | VDD | GND | VDD | GND | VDD | GND | GND | GND | GND | GND | GND | GND | GND |
„X-ray vision“ of FPGA (Die in Package)
Packaged Sample from MPW-Run
Thank You for Your Attention!