SmartHeaP – A 22nm FDX Ultra Low Power Design based on Cadence Tensilica Processor Architecture for Hearing Aid Applications

Tensilica Day, LUH IMS Hanover, Feb. 7th, 2018
SmartHeap – Project Intro

• BMBF call “New electronic systems for intelligent medical technologies (Smart Health)” managed by VDI/VDE-IT
• Previous Projects as part of the excellence cluster Hearing4All

• Project Start: April 2018
• Duration: 3 years
• Participants: Cadence, Catena, Dream Chip Technologies, Global Foundries, Fraunhofer IIS, Hoertech, Leibniz University Hannover (IMS, Prof. Blume)
Project Motivation

- Today 360 Mio. people suffer from hearing loss (that’s 5.3% of the world’s population, 9% of the kids)
- Almost 30% of elder people (>65 yrs) have a hearing loss
- Tremendous limitation of the participation in the social life
- Growing number of hearing aids users (by +30% over the last 4 years)
There is just single source hearing aid processor available as IP!
By today, none of the available DSPs is C programmable!
Time to market for new algorithms is very critical!

2016:
- 1,24 Mio. p.a. hearing aids sold in Germany
- 1,42 Bill. € revenue p.a. in Germany

2020:
SmartHeap Algorithmic Innovations (Hörtech)

• Improved fitting for hearing aids using binaural broadband signals
  → Solution: Novel binaural, bandwidth-dependent dynamic compressor (Oetting et al, 2015)

• Reduced speech intelligibility in everyday listening situations
  → Solution: Binaural localization of the target speech source (Adiloğlu et al, 2016)

• Better speech understanding in noisy environments
  → Solution: Binaural noise reduction (Gerkmann et al)
Hearing Aids Processors

- Fully programmable
- Lowest power consumption
- Not programmable

**Xtensa LX4-LX7**
Freq ~ 10-60 MHz

**ASIP**
Freq < 5-10 MHz

**Dedicated HW**
Freq < 32 KHz

**DSP ASIC**
Freq ~ 10-50 MHz

- Lee2007
- Paker2001
- Georgiou2005
- Kim2007
- Kim2008
- Mosch2000
- Park1998
- Moller1999
- Lin2006
- Chang2012
- Qiao2010
- Qiao2011
- Tensilica

Lowest power consumption

Not programmable

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Dedicated Arch.

**Fully programmable**

**Lowest power consumption**

**Not programmable**

- Power consumption (µW)
- Normalized Area (mm²)
HiFi and Fusion DSP Family

- **HiFi 3: full 32-bit Audio**
  - 4 MAC 24 and dual 32 bit architecture
  - Up to 2x performance improvement
  - Voice / noise reduction optimizations
  - Direct support for ITU intrinsics
  - 2-Way Vector FPU option

- **HiFi Extended Precision**
  - Dual 24 and single 32 bit architecture
  - Better pre and post processing
  - Improved Memory subsystem
  - Supports single core for BD, DTV

- **HiFi 2**
  - Audio and Voice optimized DSP
  - Supports 150+ audio/voice and pre/post processing packages

- **HiFi 4**
  - Quad 32x32MAC, Dual Load/Store
  - Dual 2-Way Vector FPU option
  - Performance leadership

- **Fusion**
  - 32x32 MAC, Quad 16 MAC
  - Lowest energy for IoT – Sensing, Computing, Communication

- **HiFi Mini**
  - Focus on Voice Trigger & Recognition, Voice codecs, sensor fusion, Always On functions
  - Low power & small area

- **HiFi EP**
  - 32x32 MAC, Quad 16 MAC

- **Fusion F1**
  - 32x32 MAC, Quad 16 MAC

- **32-bit ISA**
- **24-bit ISA**

- **Introduction in 2002**

- **Lower Power**
Dream Chip Technologies GmbH

Dream Chip Technologies

• Technology: 22nm FDX
• A/D: 18-20 bit@32kHz (>90dB)
• Tensilica HiFi3 with modified ISA
• Bluetooth LE for smartphone connectivity integrated
• Ultra low power design based 0.4 V libs
Work Packages

System-Level Design

• Algorithmic Design
• Mapping to SW/HW Blocks
• Technology Selection
• Power Simulation
• Performance and Area Estimation

RTL Design

• RTL Design
• IP Selection
• Power Optimization
• Verification

Implementation

• Synthesys to Gate Level
• Floorplan, Place&Route
• Further Power Optimization
• Package Design
• Prototype Design
SmartHeaP Project Schedule

- **1.04.18**: Project Start
- **30.03.19**: Algorithmic Design
- **30.09.19**: Instruction Set Optimization
- **30.03.20**: Tape Out
- **30.09.20**: Tested Samples
- **30.12.20**: Hearing Aid Prototype
SmartHeaP Partners
Thank You!

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