The KAVUAKA Hearing Aid Processor

Guillermo Payá-Vayá, Lukas Gerlach, and Holger Blume
Outline

- Digital Hearing Aid Systems
- The KAVUAKA Hearing Aid Processor
- The KAVUAKA SoC
Digital Hearing Aid Systems

- HA technology requirements
  - Small form factor (higher user acceptance)
  - Low power: \( \sim 1 \text{ mW} \) (longer battery lifetime)
  - Low processing delay: \(< 10 \text{ ms}\)
Digital Hearing Aid Systems

- HA technology requirements
  - Small form factor (higher user acceptance)
  - Low power: \( \sim 1 \text{mW} \) (longer battery lifetime)
  - Low processing delay: \(< 10 \text{ms}\)
  - Programmability / flexibility

- Performance vs. Power Consumption
  - **Programmability**
    - \( \mu \text{P} \)
    - DSP
    - ASIP
    - Dedic. HW Arch.
      - Semi-Custom
      - Custom
  - **Hardware cost efficient**

- Classification system
  - Feature extraction
  - Algorithm
    - Classification algorithm
    - Situation
      - Algorithm/parameter selection
  - Control
  - Directional microphone / omni-directional
  - Feedback suppression
  - Analysis filterbank
  - Noise reduction
  - Amplification
    - (incl. Dynamic compression)
  - Synthesis filterbank
The KAVUAKA Hearing Aid Processor (I)

- Baseline KAVUAKA Architecture

[Hartig, Payá Vayá, et al. (2014) “Customizing a VLIW-SIMD Application-Specific Instruction-Set Processor for Hearing Aid Devices”, SiPS]
The KAVUAKA Hearing Aid Processor (II)

- **Baseline KAVUAKA Architecture**
- **Parallelization Techniques**
  - SIMD / Subword Parallelism

The KAVUAKA Hearing Aid Processor (II)

- Baseline KAVUAKA Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism

The KAVUAKA Hearing Aid Processor (III)

- Baseline KAVUAKA Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)

[Payá-Vayá, et. al. (2009) "Instruction Merging to Increase Parallelism in VLIW Architectures", SoC]
The KAVUAKA Hearing Aid Processor (III)

**Assembler source code**

```
ADD V0R0, V0R2, V0R4
ADD V0R1, V0R3, V0R5
SR V1R0, V0R8, V1R2
SR V1R1, V0R9, V1R3
...
```

**Instruction scheduling**

**READ ports**

<table>
<thead>
<tr>
<th>RF0 (V0Rx)</th>
<th>RF1 (V1Rx)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register File</td>
<td>Register File</td>
</tr>
<tr>
<td>32x64-bit</td>
<td>32x64-bit</td>
</tr>
<tr>
<td>4r2w</td>
<td>4r2w</td>
</tr>
</tbody>
</table>

**WRITE ports**

- V0R8 V0R9
- V1R2 V1R3
- V1R0
- V1R1

**after scheduling**

```
(0x00) ADD V0R0, V0R2, V0R4; ADD V0R1, V0R3, V0R5
(0x01) SR V1R0, V0R8, V1R2; SR V1R1, V0R9, V1R3
```
The KAVUAKA Hearing Aid Processor (III)

Assembler source code

\[
\begin{align*}
\text{ADD}_X2 & \ V0R0+V0R1, \ V0R2+V0R3, \ V0R4+V0R5 \\
\text{SR}_X2 & \ V1R0+V1R1, \ V0R8+V0R9, \ V1R2+V1R3
\end{align*}
\]

Instruction scheduling

\[
\begin{align*}
\text{ADD}_X2 & \ V0R0+V0R1, \ V0R2+V0R3, \ V0R4+V0R5 \\
\text{SR}_X2 & \ V1R0+V1R1, \ V0R8+V0R9, \ V1R2+V1R3
\end{align*}
\]

after scheduling

\[
\begin{align*}
\text{ADD}_X2 & \ V0R0+V0R1, \ V0R2+V0R3, \ V0R4+V0R5; \\
\text{SR}_X2 & \ V1R0+V1R1, \ V0R8+V0R9, \ V1R2+V1R3; \ \text{NOP}
\end{align*}
\]
The KAVUAKA Hearing Aid Processor (III)

ADD_X2 \( V0R0+V0R1, V0R2+V0R3, V0R4+V0R5 \)
SR_X2 \( V1R0+V1R1, V0R8+V0R9, V1R2+V1R3 \)

Assembler source code

(0x00) ADD_X2 V0R0+V0R1, V0R2+V0R3, V0R4+V0R5; SR_X2 V1R0+V1R1, V0R8+V0R9, V1R2+V1R3
The KAVUAKA Hearing Aid Processor (V)

- Baseline KAVUAKA Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic using SIMD Mechanism

[Hartig, Payá-Vayá, et. al. (2014) “Customizing a VLIW-SIMD Application-Specific Instruction-Set Processor for Hearing Aid Devices” SiPS]
[Gerlach, Payá-Vayá, et al. (2016) "Efficient Emulation of Floating-Point Arithmetic on Fixed-Point SIMD Processors” SiPS]
The KAVUAKA Hearing Aid Processor (VI)

- Baseline KAVUAKA Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic
  - Complex-valued MAC

The KAVUAKA Hearing Aid Processor (VI)

- Baseline KAVUAKA Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic
  - Complex-valued MAC

<table>
<thead>
<tr>
<th>Processor: KAVUAKA</th>
<th>32 Point FFT Cycles</th>
<th>Core Area (40 nm Low Power TSMC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real-valued SIMD MAC</td>
<td>570</td>
<td>0.237 mm²</td>
</tr>
<tr>
<td>Real- and Complex-valued SIMD MAC and Butterfly Operations</td>
<td>135 (Speedup: 4.22 x)</td>
<td>0.255 mm² (Overhead: 7%)</td>
</tr>
</tbody>
</table>

# The KAVUAKA Hearing Aid Processor (VI)

<table>
<thead>
<tr>
<th>MAC Arch.</th>
<th>Name</th>
<th>Clock frequency [MHz]</th>
<th>Number of MACs</th>
<th>Word/Subword [bit]</th>
<th>FFT Points 256 [cycles]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single MAC</td>
<td>CFX [4]</td>
<td>300</td>
<td>2</td>
<td>24/24</td>
<td>8393 (438%)</td>
</tr>
<tr>
<td></td>
<td>C55x [5]</td>
<td>200</td>
<td>2</td>
<td>16/16</td>
<td>4786 (250%)</td>
</tr>
<tr>
<td></td>
<td>ADSP-21161N [6]</td>
<td>100</td>
<td>2</td>
<td>32/32</td>
<td>4316 (225%)</td>
</tr>
<tr>
<td>SIMD MAC</td>
<td>C674x [9]</td>
<td>456</td>
<td>2</td>
<td>32/32</td>
<td>2216 (116%)</td>
</tr>
<tr>
<td></td>
<td>Nadehara [10]</td>
<td>200</td>
<td>1</td>
<td>64/16</td>
<td>4093 (214%)</td>
</tr>
<tr>
<td></td>
<td>SC3850 [11]</td>
<td>1000</td>
<td>4</td>
<td>64/16</td>
<td>2587 (135%)</td>
</tr>
<tr>
<td>SIMD CMAC</td>
<td>KAVUAKA</td>
<td>50</td>
<td>1</td>
<td>64/32</td>
<td>1915 (100%)</td>
</tr>
</tbody>
</table>

The KAVUAKA Hearing Aid Processor (VII)

- **Baseline KAVUAKA Architecture**
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)

- **Parallelization Techniques**
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)

- **Specialization Techniques**
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic
  - Complex-valued MAC
  - RF Isolation and Forwarding

The KAVUAKA Hearing Aid Processor (VII)

Register File (2 x 32 Register)

Bank 0  
V0-V31

Bank 1  
V0-V31

The KAVUAKA Hearing Aid Processor (VII)

Register File (2 x 32 Register)

Bank 0

Bank 1

V0-V31

V0-V31

4R 2W Ports

Address

Enable

Address Isolation
The KAVUAKA Hearing Aid Processor (VII)

Register File (2 x 32 Register)

4R 2W Ports

Address Isolation

Bank 0

V0-VX

Bank 1

V0-VX

Configurable Dummy Registers

VX-V31

VX-V31
The KAVUAKA Hearing Aid Processor (VII)

Register Access Stage

Register File (2 x 32 Register)

Bank 0

V0-VX

Bank 1

V0-VX

Configurable Dummy Registers

VX-V31

VX-V31

Execution Stage

Pipeline

Register

Address Compare

Use of Forwarding Registers

Write Back Paths

MUL

4R 2W Ports

Address

Enable

Address Isolation
The KAVUAKA Hearing Aid Processor (VII)

Adaptive Gain
Beamformer

<table>
<thead>
<tr>
<th>Bit Width</th>
<th>Ref. register file</th>
<th>Ref. register file + isolation</th>
<th>Ref. register file + isolation + dummy</th>
</tr>
</thead>
<tbody>
<tr>
<td>24 bit</td>
<td>100   91  83</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32 bit</td>
<td>100   95  90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>48 bit</td>
<td>100   94  91</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64 bit</td>
<td>100   93  90</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

40 nm Low Power TSMC
The KAVUAKA Hearing Aid Processor (VIII)

- Baseline KAVUAKA Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic
  - Complex-valued MAC
  - RF Isolation and Forwarding
  - Co-processors

The KAVUAKA Hearing Aid Processor (VIII)

- **Baseline KAVUAKA Architecture**
- **Parallelization Techniques**
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- **Specialization Techniques**
  - Complex Addressing Mode

Fast computations of non-linear functions

<table>
<thead>
<tr>
<th>Hyperbolic and trigonometric operations</th>
<th>Sine</th>
<th>Cosine</th>
<th>Exponential</th>
<th>Natural logarithm</th>
<th>Square root</th>
</tr>
</thead>
<tbody>
<tr>
<td>KAVUAKA+CORDIC (HW)</td>
<td>71</td>
<td>71</td>
<td>76</td>
<td>56</td>
<td>59</td>
</tr>
<tr>
<td>KAVUAKA (SW)</td>
<td>621</td>
<td>621</td>
<td>668</td>
<td>664</td>
<td>649</td>
</tr>
<tr>
<td>TI TMS320C6478</td>
<td>1259</td>
<td>1523</td>
<td>1529</td>
<td>1134</td>
<td>341</td>
</tr>
</tbody>
</table>

The KAVUAKA Hearing Aid Processor (IX)

- **Baseline KAVUAKA Architecture**
- **Parallelization Techniques**
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- **Specialization Techniques**
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic using SIMD Mechanism
  - Complex-valued MAC
  - RF Isolation and Forwarding
  - Co-processors
  - Low latency audio interface

The KAVUAKA Hearing Aid Aid Processor (X)
A Digital Hearing Aid Application-Specific Processor

- KAVUAKA Processor (Big Configuration)
  - VLIW: 2-issue-slots (+ 2 instruction merging)
  - SIMD: 64-bit or 2x32-bit or 4x16-bit or 8x8-bit
  - Max. Frequency: 75 MHz
  - TSMC 40 nm Low Power Technology
  - Estimated Silicon Area: 0.922 mm² < 1 mm²
  - Estimated Power Consumption: 0.635 mW < 1 mW

- Test Chip
  - Available Silicon Area: 3.9 mm²
  - 2 Cluster each with 2 KAVUAKA and 10 Co-Processors
The manufacturing is scheduled within the next possible tape-out run, which is expected to take place 06/03/2018 and manufactured on 05/04/2018.
Thank you for the attention!