IMS
Institute of Microelectronic Systems

3rd Tensilica Day – Trends in Modern Design of Configurable Processors

Institute of Microelectronic Systems

Welcome		**9:00**
9:00	Welcome	*Blume, Klotz (LUH, Cadence)*
Session1 - *Tutorials*		**9:15 – 12:00**
9:15	Tensilica 2018. What's New?	*Binning (Cadence)*
10:00	***Coffee break***	
10:30	Pedestrian Detection Demo with Tensilica IVP DSP on Protium FPGA-based prototype (Tutorial + Demo)	*Wegner (Cadence)*
Lunch and Trends		**12:00 – 13:00**
	Fingerfood, Posters and Demonstrators	
Session on Technology, Architectures and Tools		**13:00–15:15**
13:00	Application/Hardware-Aware Operating System Design	*Dietrich (SRA, LUH)*
13:20	Tbd. (ASIP Video Processing Architecture Videantis)	*Stolberg (Videantis)*
13:40	Self-Adaptive Multiprocessor Systems-on-Chip	*Göhringer (TUD)*
14.00	The KAVUAKA Hearing Aid Processor	*Payá-Vayá (IMS, LUH)*
14.20	FDX-Technology for Digital-SOC and Analog-RF system integration	*Teepe (Globalfoundries)*
Coffee Break		**14:40 – 15:00**
Session on ASIP-Case Studies		**15:00–16:20**
15:00	Run-Time Reconfigurable Processor Architectures for Embedded Systems	*Hübner (RUB)*
15:20	Best Practice Design Experience with a Multiprocessor Tensilica Chip Architecture for Automotive Applications	*Zeller (DreamChip)*
15:40	SmartHeaP – A 22nm FDX Ultra Low Power Design based on Cadence Tensilica Processor Architecture for Hearing Aid Applications	*Benndorf (DreamChip)*
16:00	Low-Power Implementation of CNN-based Object-Detection on Tensilica Vision Series DSPs	*Behmann (IMS, LUH)*
Closing		**16:20**