4th Tensilica Day – Trends in Modern Design of Configurable Processors
Day 1 – 23rd September 2019

Welcome & Introduction
14:00 Welcome
Holger Blume
Institute of Microelectronic Systems, Leibniz University Hannover

14:15 Tensilica 2019. What’s New?
Cadence

Coffee Break
15:00

Session 1 Neural Network Acceleration
15:15 Configurable Processing Elements for Flexible Acceleration of Variable Precision Neural Networks
Nael Al-Fasfous
Chair of Integrated Systems, TU Munich

15:45 CNN Inference on Coarse-Grain Reconfigurable Arrays under Throughput Constraints
Christian Heidorn
HW/SW Co-Design, Dep. of Computer Science, FAU Erlangen-Nürnberg

16:15 A Power Efficient Network Coding Accelerator
Mattis Hasler
Vodafone Chair, Mobile Communication Systems, TU Dresden

Coffee Break
16:45

Session 2 Theory & Software Tooling
17:00 Exploration of Memory Energy-Reduction Strategies for a Deep Learning ASIP
Lennart Reimann
Institute for Communication Technologies & Embedded Systems, RWTH Aachen

17:30 Evaluation and optimization of a Tensilica processor for hearing aids
Jens Karrenbauer
Institute of Microelectronic Systems, LU Hannover

Welcome Reception & Networking
18:00–20:00
4th Tensilica Day – Trends in Modern Design of Configurable Processors  
Day 2 – 24th September 2019

Welcome & Introduction 9:00

9:00  Welcome  
Holger Blume  
Institute of Microelectronic Systems, Leibniz University Hannover

9:15  Emulation Tutorial  
Cadence

Coffee Break 10:15

Session 3  Industrial ASIP Applications 10:30

10:30  New general purpose FPGA with novel architecture  
Michael Gude  
Cologne Chip

11:00  Structure from motion on Tensilica Vison P6  
Christoph Heinrichs  
Dream Chip Technologies GmbH

11:30  A unified visual computing platform  
Hans-Joachim Stolberg  
videantis GmbH

Lunch and Trends 12:00

1  Protium Emulation System Demonstration with Tensilica DSP  
Cadence

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Keynote 13:00

13:00  Next Generation Neuro Science Simulation Systems  
Tobias G. Noll  
Chair of Integrated Digital Systems and Circuit Design, RWTH Aachen

Coffee Break 13:45

Session 4  ASIP Case-Studies I 14:00

14:00  t.b.a.  
Michael Hübner  
Chair of Computer Engineering, BTU Cottbus

14:30  InterSloth: Global Hardware-Based Scheduling in a Multi-Core RTOS on RISC-V  
Christian Dietrich  
Systems Research and Architecture Group, Leibniz University Hannover

15:00  Energy Efficient GFDM Accelerator for Users Devices  
Robert Wittig  
Vodafone Chair, Mobile Communication Systems, TU Dresden

Coffee Break 15:30
Session 5  ASIP Case-Studies II

15:45  Application Specific Memory Controller
Norbert Wehn  Division of Microelectronic Systems Design, TU Kaiserslautern

16:15  Application-Specific Soft-Core Vector Processor for Advanced Driver Assistance Systems
Guillermo Payá Vayá  Institute of Microelectronic Systems, LU Hannover

16:45  t.b.a.
Alberto García-Ortiz  Chair for Integrated Digital Systems, TU Bremen

Closing  17:15–17:30