Solutions for Chapter 3

Exercise 3.1

a. Input b_i has to be complemented.

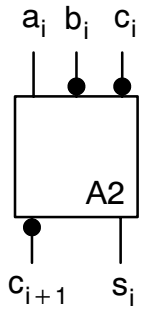
a_n	b_n	c_n	$\overline{b_n}$	c_{n+1}	s	
0	0	0	1	0	1	p
0	0	1	1	1	0	p
0	1	0	0	0	0	k
0	1	1	0	0	1	k
1	0	0	1	1	0	g
1	0	1	1	1	1	g
1	1	0	0	0	1	p
1	1	1	0	1	0	p

$$s_i = a_i \oplus \overline{b}_i \oplus c_i$$

$$c_{i+1} = a_i\overline{b}_i \vee a_i c_i \vee \overline{b}_i c_i$$

b. The Signals b_i, c_i and c_{i+1} have negative weights.

a_n	(b_n)	(c_n)	(c_{n+1})	s	
0	0	0	0	0	p
0	0	1	1	1	p
0	1	0	1	1	g
0	1	1	1	0	g
1	0	0	0	1	k
1	0	1	0	0	k
1	1	0	0	0	p
1	1	1	1	1	p



c_{i+1} \ a_ib_i	00	01	11	10
0	0	1	0	0
1	1	1	1	0

s_i \ a_ib_i	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$s_i = \overline{a}_i\overline{b}_i c_i \vee \overline{a}_i b_i \overline{c}_i \vee a_i\overline{b}_i\overline{c}_i \vee a_i b_i c_i$$

$$= a_i \oplus b_i \oplus c_i$$

$$c_{i+1} = \overline{a}_i b_i \vee \overline{a}_i c_i \vee b_i c_i$$

c. Both implementation deliver the same bit pattern. The interpretation of the bit pattern, the numeric representation, depends on the numeric representation of the input operands.
If both input operands are positive dual numbers and the result has the same length n as the input operands, the result can be interpreted as a positive dual number as long as the first operand is always larger than or equal to the second operand. If in this case the first is at maximum by $2^{n-1} - 1$ larger than the second operand or the second at maximum by 2^{n-1} larger than the first, the result can be interpreted as a two's compement number.
In case of a wider result, yielded by a wider subtractor and extended input operands, the result can be interpreted as a two's complement number.

d. a.:
$$g_i = a_i\overline{b}_i$$

$$p_i' = a_i \vee \overline{b}_i \;;\; p_i = a_i \oplus \overline{b}_i$$

$$c_{i+1} = g_i \vee p_i c_i$$

$$s_i = p_i \oplus c_i$$

b.:
$$g_i = \overline{a}_i b_i$$

$$p_i' = \overline{a}_i \vee b_i \;;\; p_i = \overline{a}_i \oplus b_i$$

$$s_i = \overline{p}_i \oplus c_i$$

e. Except for changed connections of the signalpairs $b_i, \overline{b}_i$, $a_i, \overline{a}_i$ and $p_i, \overline{p}_i$, the structure of both implementations is identical. As a consequence, the transistor count and the circuit delay are the same.

Exercise 3.2

a. Delay NAND gate:

NAND m: $T_{D,HL} = m(2+F)\tau_L$

$T_{D,LH} = (2+F)\tau_L$

INV = NAND 1

Assumption: $C_I = 2C_{L,0}$

Carry path of a full adder

$$T_{D,VA,cc} = T_{D,NAND2,LH} + T_{D,NAND3,HL}$$
$$= (2+1)\tau_L + 3(2+F_c)\tau_L = (9+3F_c)\tau_L$$
$$T_{0,cc} = 9\tau_L; \quad T_{1,cc} = 3\tau_L$$

Sum path of a full adder

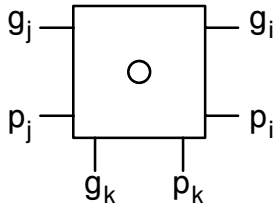
$$T_{D,VA,cs} = T_{D,INV} + T_{D,NAND3,LH} + T_{D,NAND4,HL}$$
$$= (2+2)\tau_L + (2+1)\tau_L + 4\,(2+F_s)\tau_L$$
$$= (15+4F_s)\tau_L$$
$$T_{0,cs} = 15\,\tau_L; \quad T_{1,cs} = 4\,\tau_L$$

T_0 describes the load independent part of the delay. T_1 describes the load dependend part, normalized to a fan−out factor of 1.

b. Bit−Slice Adder

$$T_{D,ADD} = (n-1)T_{0,CC} + T_{0,cs}$$
$$T_{D,ADD} = (9n+6)\tau_L$$

Lookahead−Carry−Operator



$$(g_i, p_i) = (g_j, p_j) \circ (g_k, p_k)$$
$$= (g_j \vee p_j g_k, p_j p_k)$$

$$T_{D,OP} = T_{0,OP} + T_{1,OP}\,F$$

$$= \begin{cases} (7 + 2F)\tau_L & HL \quad g_k \rightarrow g_i \\ (8 + F)\tau_L & LH \quad g_k \rightarrow g_i \end{cases}$$

Critical path of the carry block:

$$(g_0, p_0) \rightarrow (G_{n-2}, P_{n-2})$$

Number of operators in critical path: $2\log\frac{n}{2}$

$$T_{D,Carry-Block} = 2\log\frac{n}{2} T_{0,OP}$$

$$= (2\log n - 2)\, T_{0,OP}$$

c. Bit–Slice Adder
Fan–in of one full adder input: 5

$$T_{D,ADD} = (n-1)F_c\, T_{1,cc} + T_{1,cs}\, F_s$$

$$F_c = 5 \text{ (Fan–Out Carry)}$$

$$T_{D,ADD} = (n-1) \cdot 15\,\tau_L + 4\,\tau_L F_s$$

Carry block of look–ahead carry adder:

Load of stage j:

binary tree: 2 + j

inverse binary tree; j

$$T_{D,Carry-Block} = \sum_{j=1}^{\log_2^n} [T_{1,OP}\,(2 + j) + T_{1,OP} j]$$

$$= 2T_{1,OP} \sum_{j=1}^{\log_2^n} (1 + j)$$

$$\sum_{j=1}^{\log_2^n} (1 + j) = \log\frac{n}{2} + \frac{1}{2}\log\frac{n}{2}(1 + \log\frac{n}{2})$$

$$= \frac{1}{2}\log^2 n + \frac{1}{2}\log n - 1$$

$$T_{D,Carry-Block} = (\log^2 n + \log n - 2)\, T_{1,OP}$$

d. The delay characteristic of a circuit model may vary depending on the complexity of the model. In this example, the load neglecting model and the model

taking loads into account both show the same topology of the critical path. However, the consideration of the load leads to a totally different order of the delay characteristics for the binary look–ahead carry adder. Only as long as all outputs of all gates drive loads such that the delay of each gate is scaled by the same factor, the overall delay characteristics of both models can be safely assumed to be the same.

Exercise 3.3

a. **Function** F_α

$$(GG_j, GP_j) = (g_{4j+3}, p_{4j+3}) \circ (g_{4j+2}, p_{4j+2}) \circ (g_{4j+1}, p_{4j+1}) \circ (g_{4j}, p_{4j})$$

$$GG_j = g_{4j+3} \vee p_{4j+3}\, g_{4j+2} \vee p_{4j+3}\, p_{4j+2}\, g_{4j+1} \vee p_{4j+3}\, p_{4j+2}\, p_{4j+1}\, g_{4j}$$

$$GP_j = p_{4j+3}\, p_{4j+2}\, p_{4j+1}\, p_{4j}$$

Function F_β

$$(G_{4m+k}, P_{4m+k}) = (g_{4m+k}, p_{4m+k}) \circ (G_{4m+k-1}, P_{4m+k-1})$$

$$G_{4m} = g_{4m} \vee p_{4m}\, G_{4m-1}$$

$$P_{4m} = p_{4m}\, P_{4m-1}$$

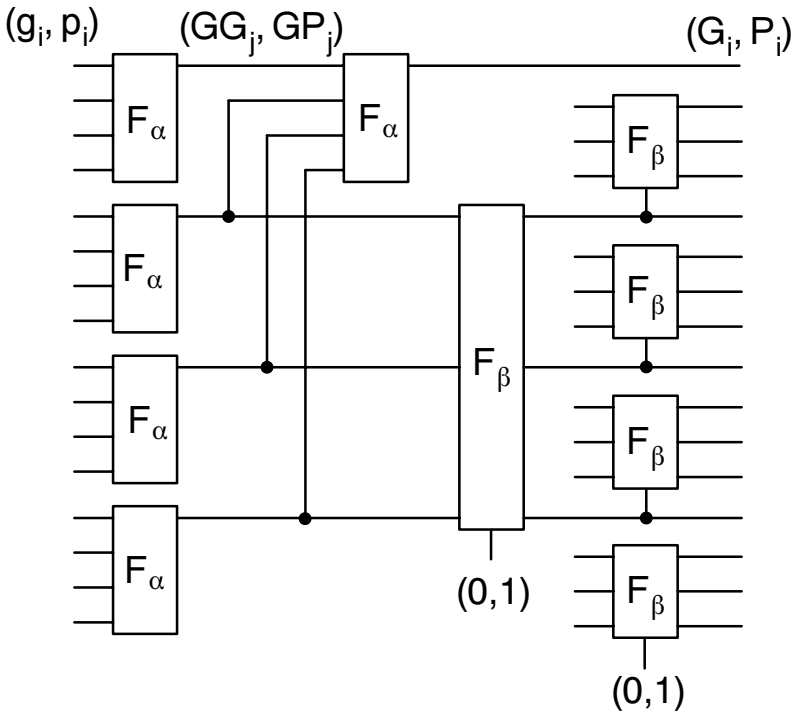
$$G_{4m+1} = g_{4m+1} \vee p_{4m+1}\, g_{4m} \vee p_{4m+1}\, p_{4m} G_{4m-1}$$

$$P_{4m+1} = p_{4m+1}\, p_{4m}\, P_{4m-1}$$

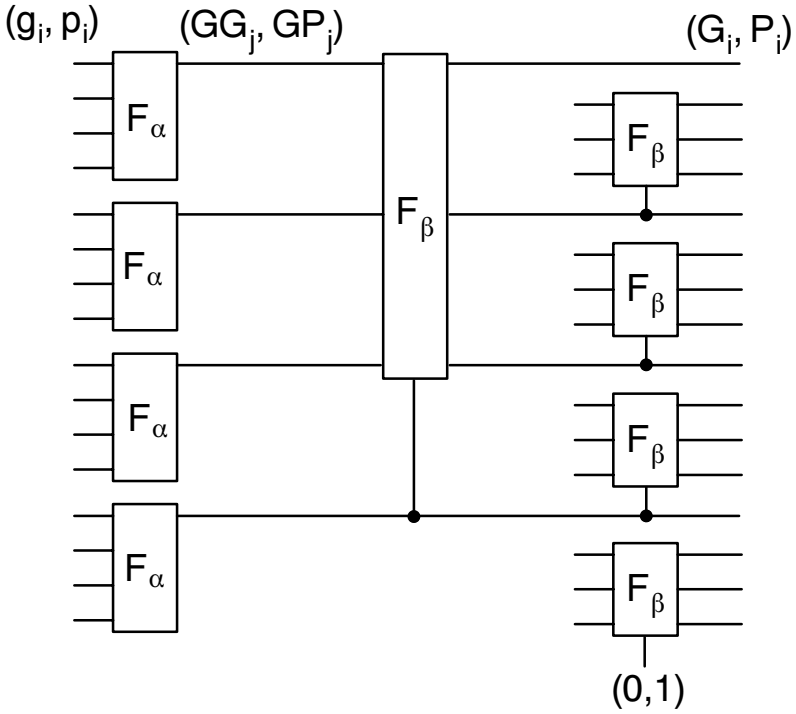
$$G_{4m+2} = g_{4m+2} \vee p_{4m+2}\, g_{4m+1} \vee p_{4m+2}\, p_{4m+1}\, g_{4m} \vee p_{4m+2}\, p_{4m+1}\, p_{4m}\, G_{4m-1}$$

$$P_{4m+2} = p_{4m+2}\, p_{4m+1}\, p_{4m}\, P_{4m-1}$$

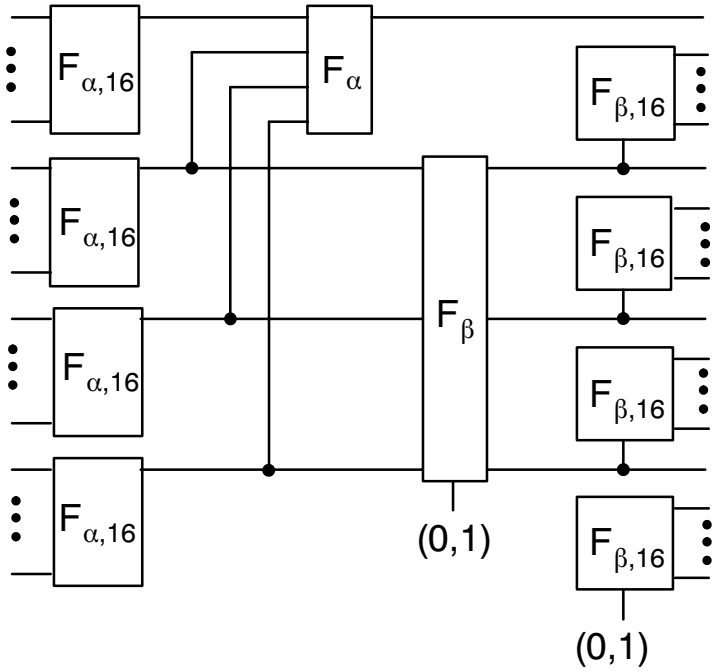
b. 16 bit adder: $F_{\alpha,16}$, $F_{\beta,16}$



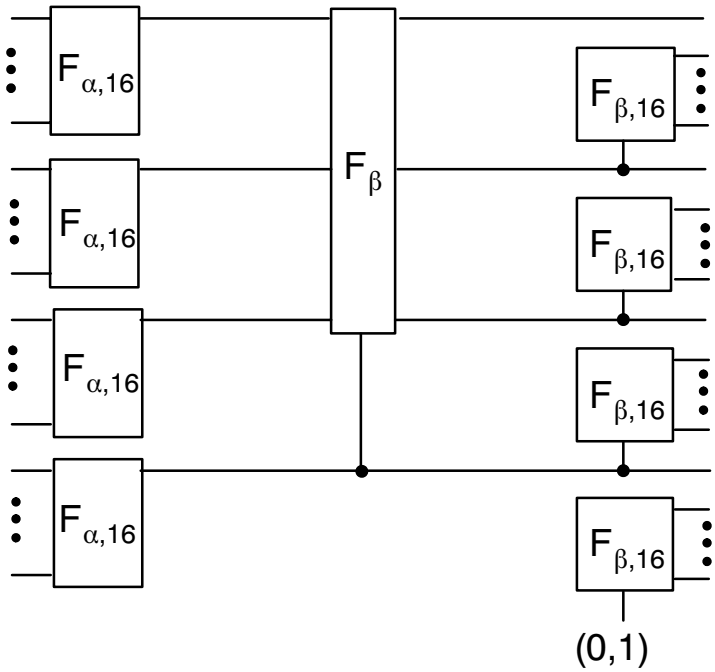
Alternative Solution (not considered in the following delay/transistor count calculations):



64 bit adder



Alternative Solution (not considered in the following delay/transistor count calculations):



c. Binary–Lookahead–Carry: $2\log_2 n - 1$
Quartarnary – Lookahead–Carry: $2\log_4 n$

d. Transistor count:
Binary–Lookahead–Carry:
Operator: 3 NAND2, 2 INV; $n_{Tr} = 16$

n	n_{OP}	N_{Tr}
4	4	64
16	26	416
64	120	1920

Quartarnary–Lookahead–Carry:
F_α: 3 NAND4, NAND3, NAND2, 2INV; $n_{Tr} = 38$
F_β: 3 NAND4, 4NAND3, 5NAND2, 6INV; $n_{Tr} = 80$

n	n_α	n_β	N_{Tr}
4	1	1	118
16	5	5	590
64	21	21	2478

Delay:

Binary–Lookahead–Carry:
Operator: $T_{D,OP} = (7 + 2F)\tau_L$
Critical Path

n	n_{OP}	Load F	T_D/τ_L
4	2	3,1	22
16	6	3,4,5,3,2,1	78
64	10	3,...,7,5,...,1	150

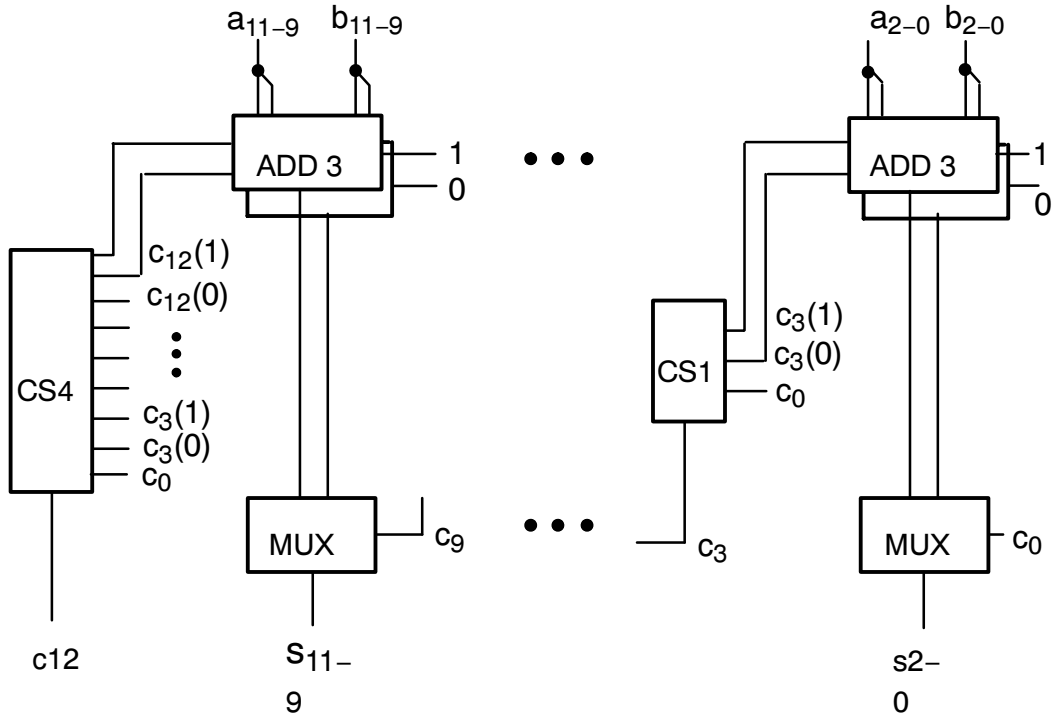
Quartarnary–Lookahead–Carry:
F_α: $T_{D,\alpha} = (11 + 4F)\,\tau_L \quad F_{in} = 1$
F_β: $T_{D,\beta} = (11 + 4F)\,\tau_L \quad F_{in} = 3$
Critical path

n	n_α	Load F	n_β	Load F	T_D/τ_L
4			1	1	15
16	1	4	2	4,1	69
64	2	4,4	3	7,4,1	135

Increased loads for $(g_i\,, p_i)$ and differences between LH and HL transitions are not considered.

Exercise 3.4

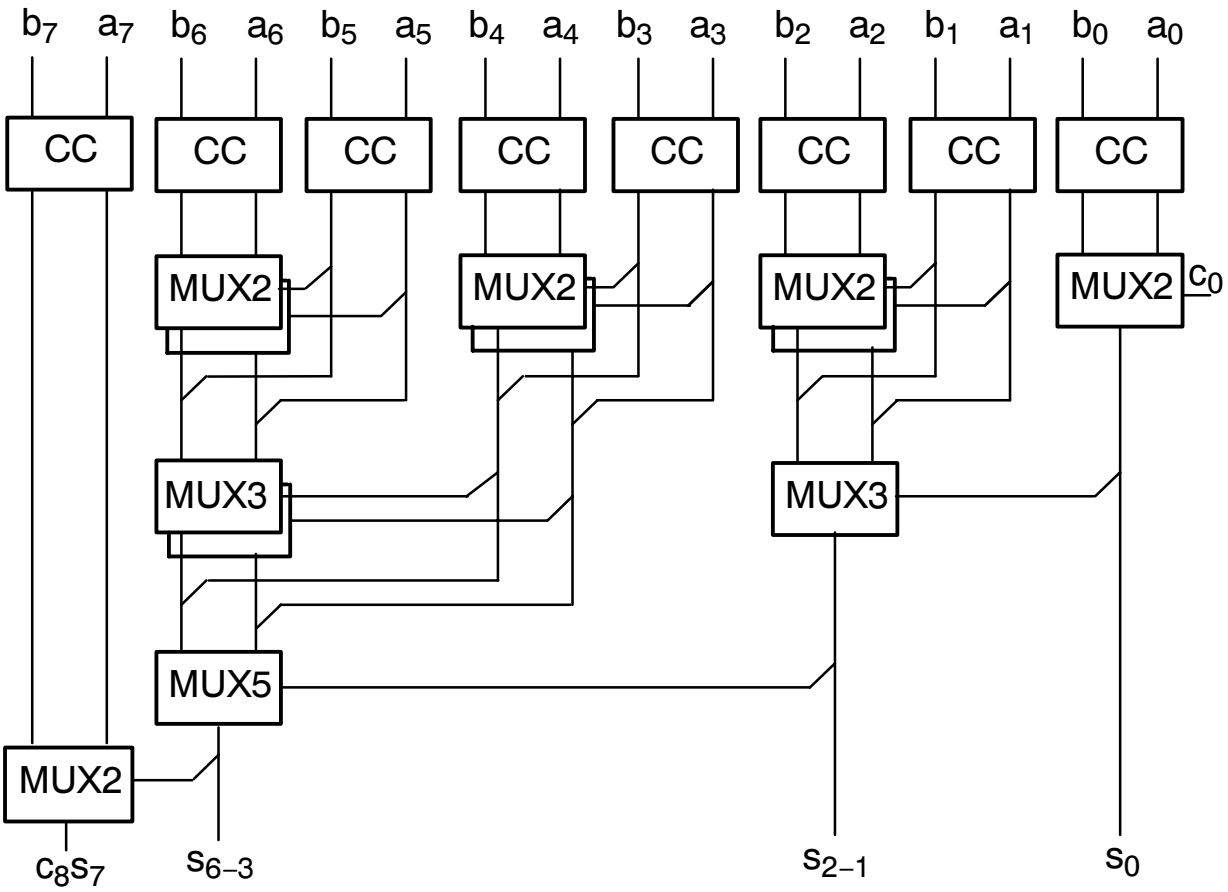
a.



b. CS1: $c_3 = c_3(0) \vee c_3(1)c_0$
CS2: $c_6 = c_6(0) \vee c_6(1)\, c_3(0) \vee c_6(1)\, c_3(1)\, c_0$
CS3: $c_9 = c_9(0) \vee c_9(1)\, c_6(0) \vee c_9(1)\, c_6(1)\, c_3(0) \vee c_9(1)\, c_6(1)\, c_3(1)\, c_0$
CS4: $c_{12} = c_{12}(0) \vee \ldots \vee c_{12}(1)\, c_9(1)\, c_6(1)\, c_3(1)\, c_0$

Exercise 3.5

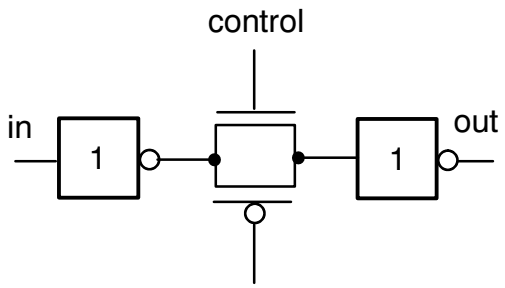
a.



i	7	6	5	4	3	2	1	0
a_i	1	1	0	0	1	1	1	0
b_i	1	1	0	1	1	0	0	1
$s_i(0)$	0	0	0	1	0	1	1	1
$c_{i+1}(0)$	1	1	0	0	1	0	0	0
$s_i(1)$	1	1	1	0	1	0	0	
$c_{i+1}(1)$	1	1	0	1	1	1	1	
$s_i(0)$		0	0	0	0	1	1	1
$c_{i+1}(0)$		1		1		0		0
$s_i(1)$		0	1	0	1	0	0	
$c_{i+1}(1)$		1		1		1		
$s_i(0)$		0	1	0	0	1	1	1
$c_{i+1}(0)$		1				0		
$s_i(1)$		0	1	0	1			
$c_{i+1}(1)$		1						
$s_i(0)$	0	0	1	0	0	1	1	1
$c_{i+1}(0)$	1	1						
$s_i(1)$	1							
$c_{i+1}(1)$	1							
s_i	1 0	0	1	0	0	1	1	1

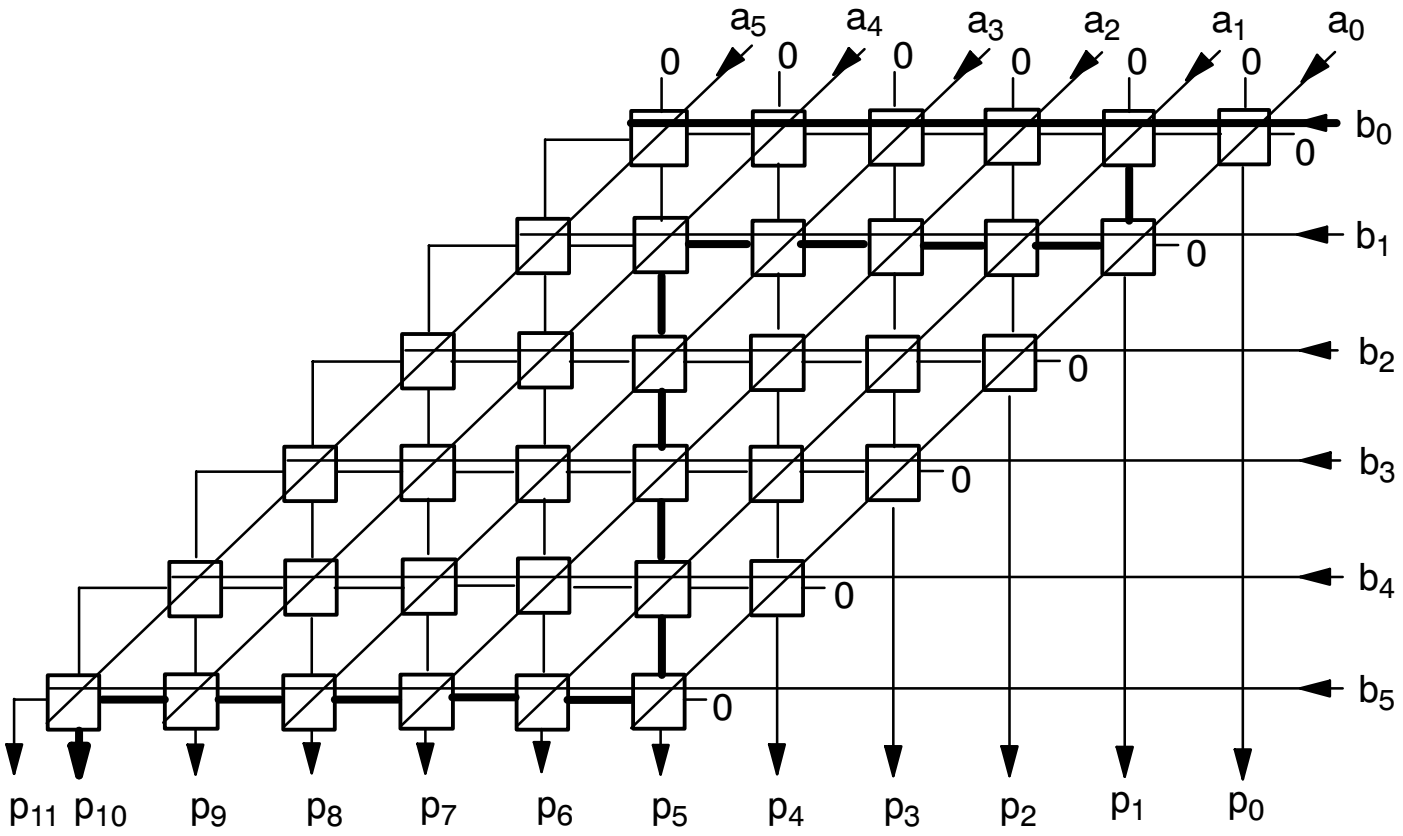
b. The result of the CC cell of the lowest significant bit slice can be used directly. In fact, a half adder can replace that cell.

c. To break up transmission gate chains in multiplexer implementations, buffers should be used.



Exercise 3.6

a.

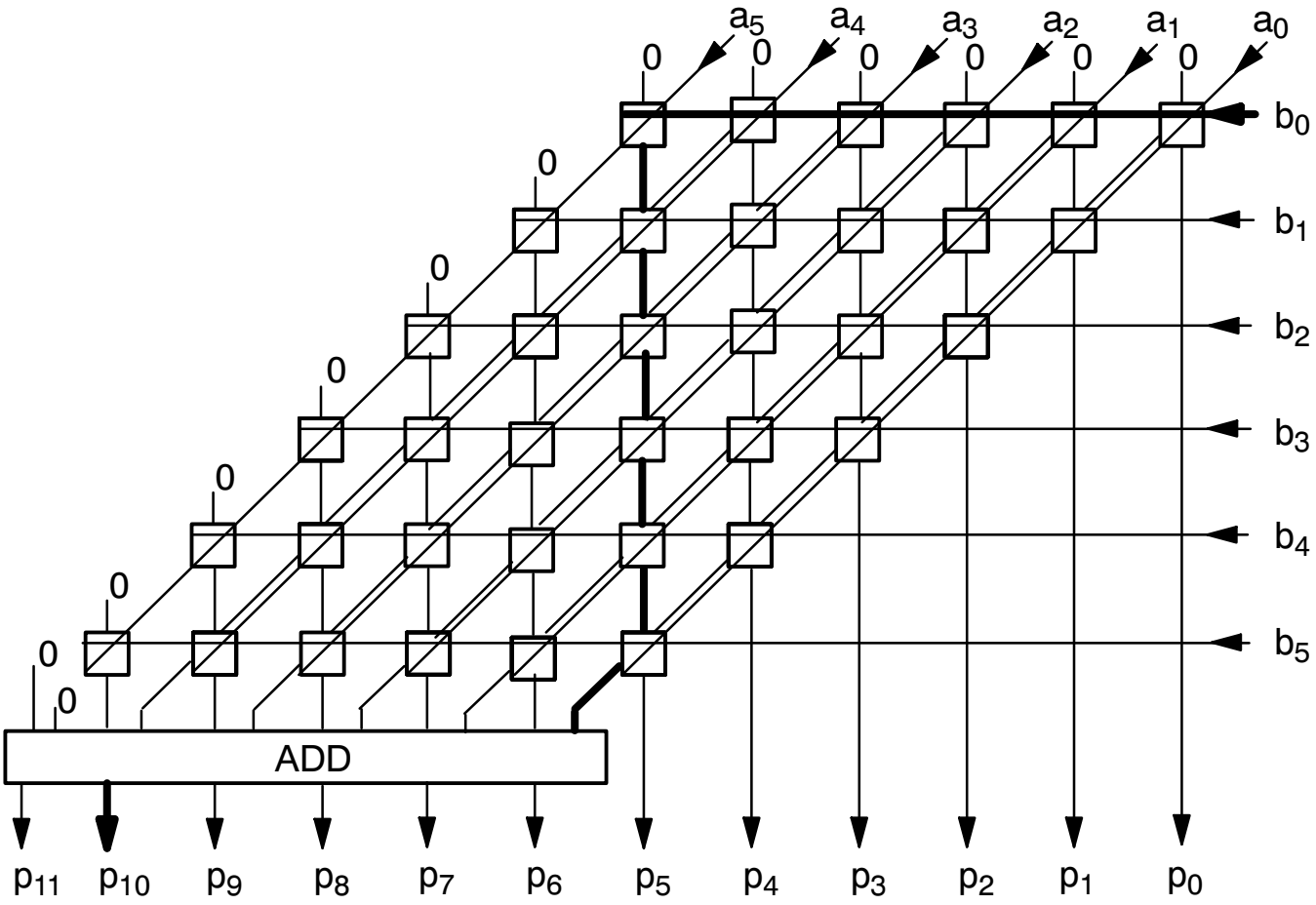


Delay:

$T_D = T_{D,AND} + T_{D,FA,c',s} + T_{D,FA,c',c}(n-3) + T_{D,FA,c',s}$
$+ T_{D,FA,s',s}(n-3) + T_{D,FA,s',c} + T_{D,FA,c',c}(n-2) + T_{D,FA,c',s}$
$= (4n-5)T_0$

Operands for worst case delay:
(assuming inputs are initially zero)
$A = 111111,\ B = 111111$

b.



Delay:

$T_D = T_{D,AND} + T_{D,FA,s',s}(n-2) + T_{D,FA,s',c} + T_{D,FA,c',c}(n-2) + T_{D,FA,c',s}$

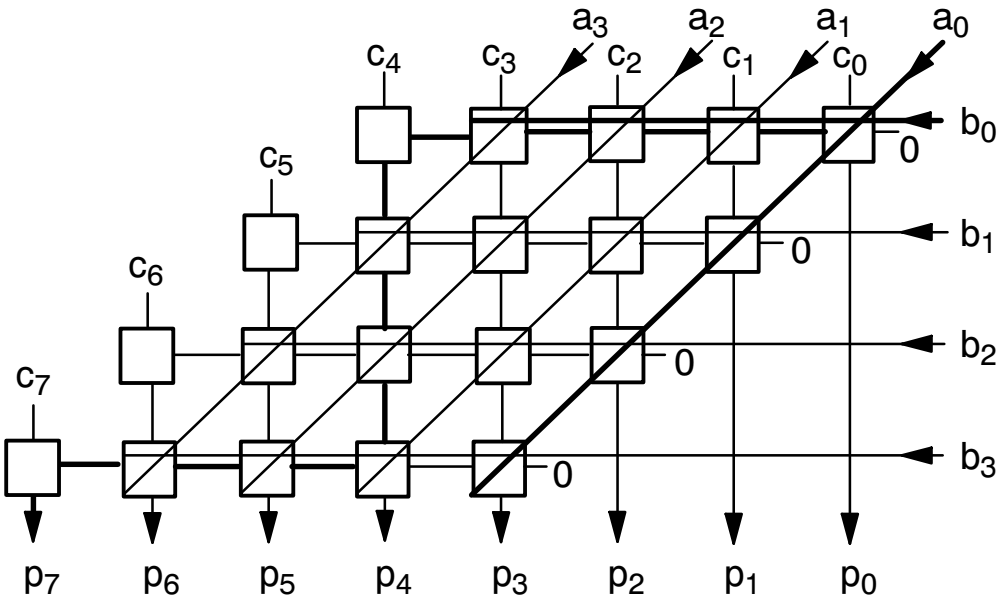
$= (3n-2)T_0$

Operands for worst case delay:
(assuming inputs are initially zero)

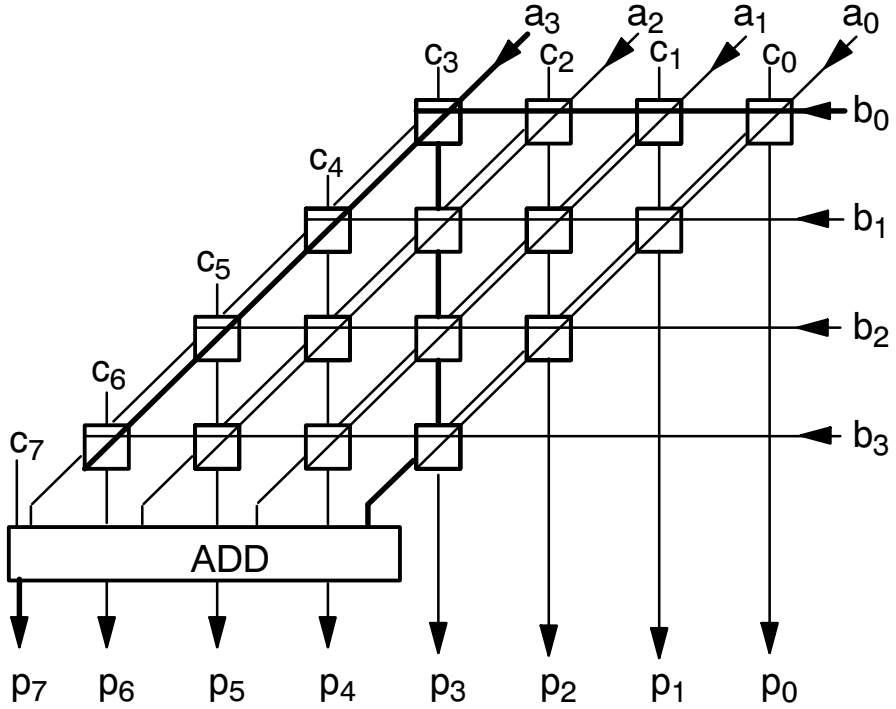
$A = 111111,\ B = 111111$

Exercise 3.7

a.



b.



c.

Delay of the ripple carry multiplier/adder:

$T_D = T_{D,AND} + T_{D,FA,s',c} + 3T_{D,FA,c',c} + T_{D,FA,c',s}$
$+ 2T_{D,FA,s',s} + T_{D,FA,s',c} + 2T_{D,FA,c',c} + T_{D,FA,c',s}$
$= 7.5T_S$

Delay of the carry save multiplier/adder:

$T_D = T_{D,AND} + 3T_{D,FA,s',s} + T_{D,FA,s',c} + 3T_{D,FA,c',c} + T_{D,FA,c',s}$
$= 6T_S$

Exercise 3.8

a.

4 bit counter;

$$s_0 = a \oplus b \oplus c \oplus d$$

$$s_1 = (a \vee b \vee c)\,(a \vee b \vee d)\,(a \vee c \vee d)\,(b \vee c \vee d)\,(\overline{a} \vee \overline{b} \vee \overline{c} \vee \overline{d})$$

$$s_2 = a\,b\,c\,d$$

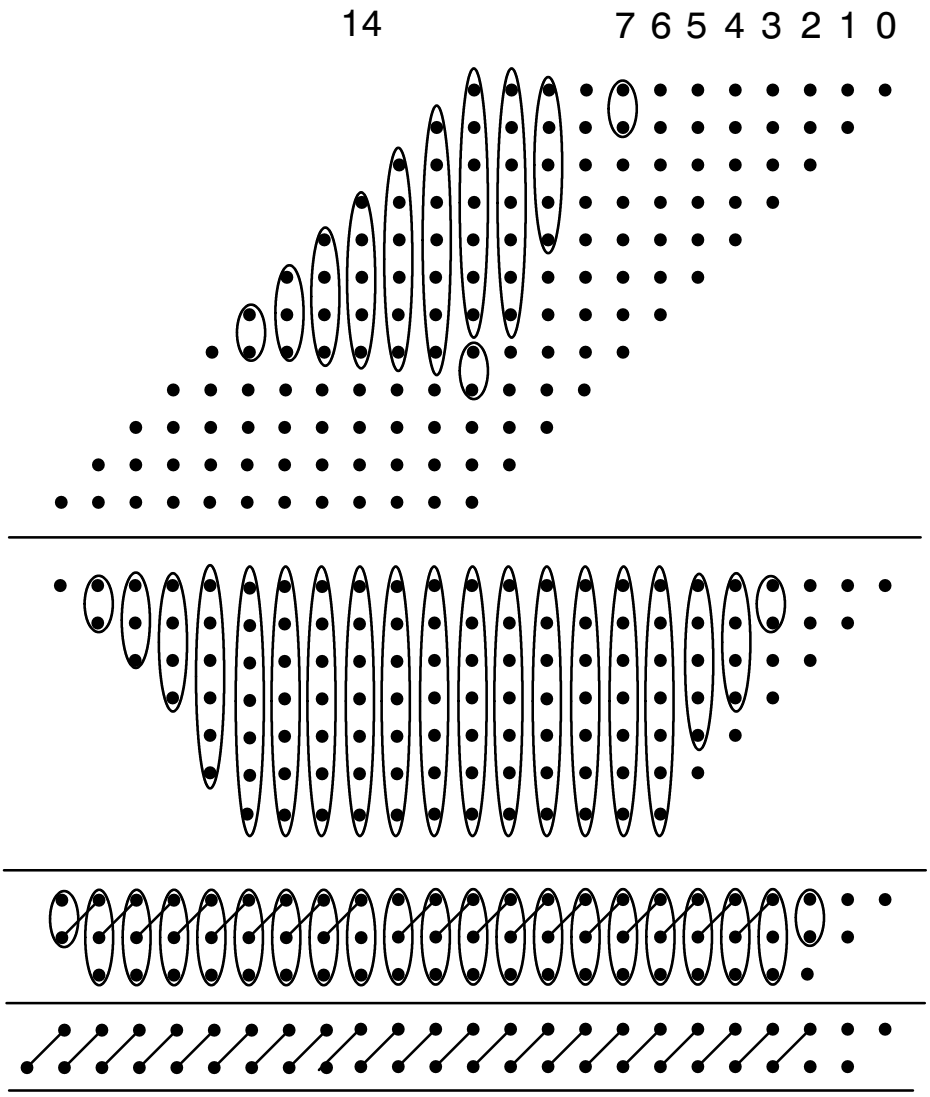
5 bit counter:

$$s_0 = a \oplus b \oplus c \oplus d \oplus e$$

$$\begin{aligned} s_1 = {} & (a \vee b \vee c \vee d)\,(a \vee b \vee c \vee e)\,(a \vee b \vee d \vee e)\,(a \vee c \vee d \vee e) \\ & (b \vee c \vee d \vee e)\,(\overline{a} \vee \overline{b} \vee \overline{c} \vee \overline{d})\,(\overline{a} \vee \overline{b} \vee \overline{c} \vee \overline{e}) \\ & (\overline{a} \vee \overline{b} \vee \overline{d} \vee \overline{e})\,(\overline{a} \vee \overline{c} \vee \overline{d} \vee \overline{e})\,(\overline{b} \vee \overline{c} \vee \overline{d} \vee \overline{e}) \end{aligned}$$

$$s_2 = a\,b\,c\,d \vee a\,b\,c\,e \vee a\,b\,d\,e \vee a\,c\,d\,e \vee b\,c\,d\,e \vee$$

b.



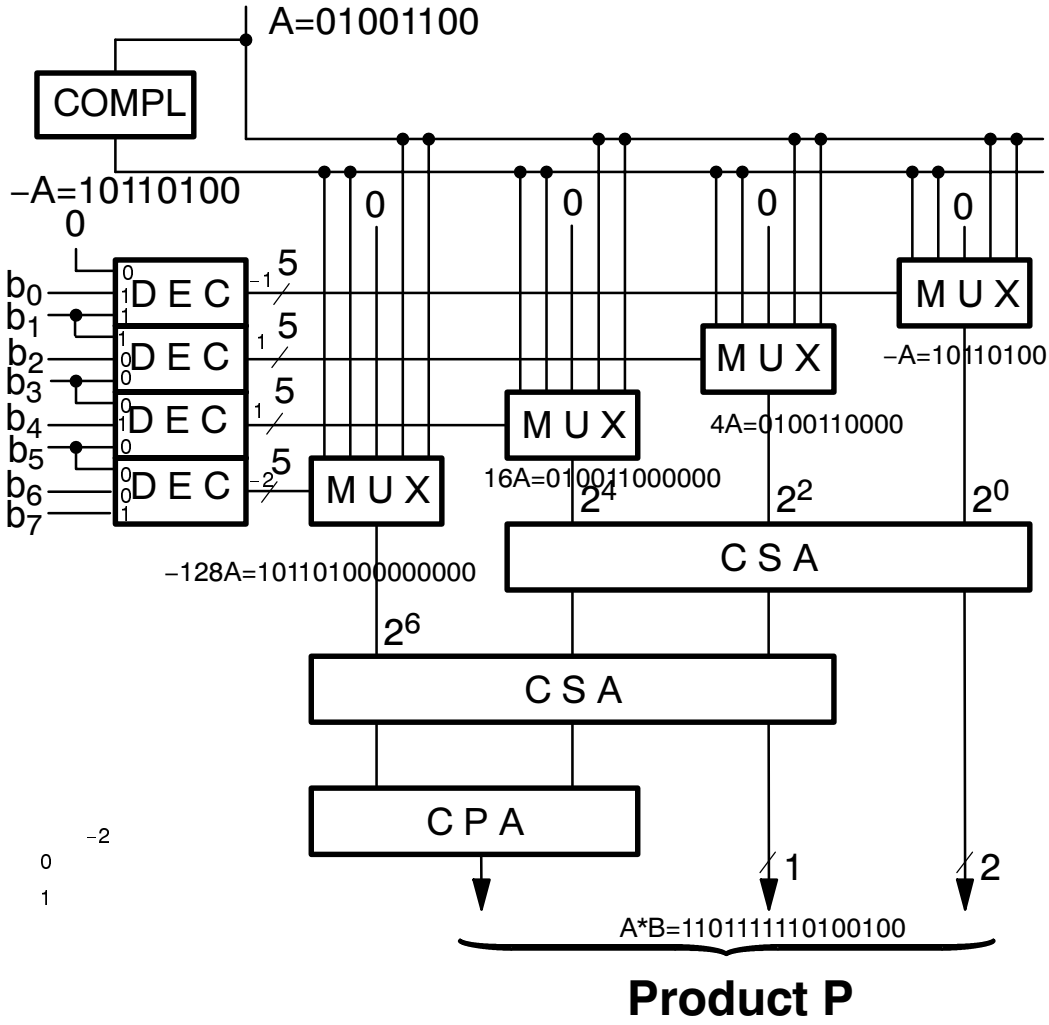
stage	# operands
3	12
2	7
1	3
0	2

c.

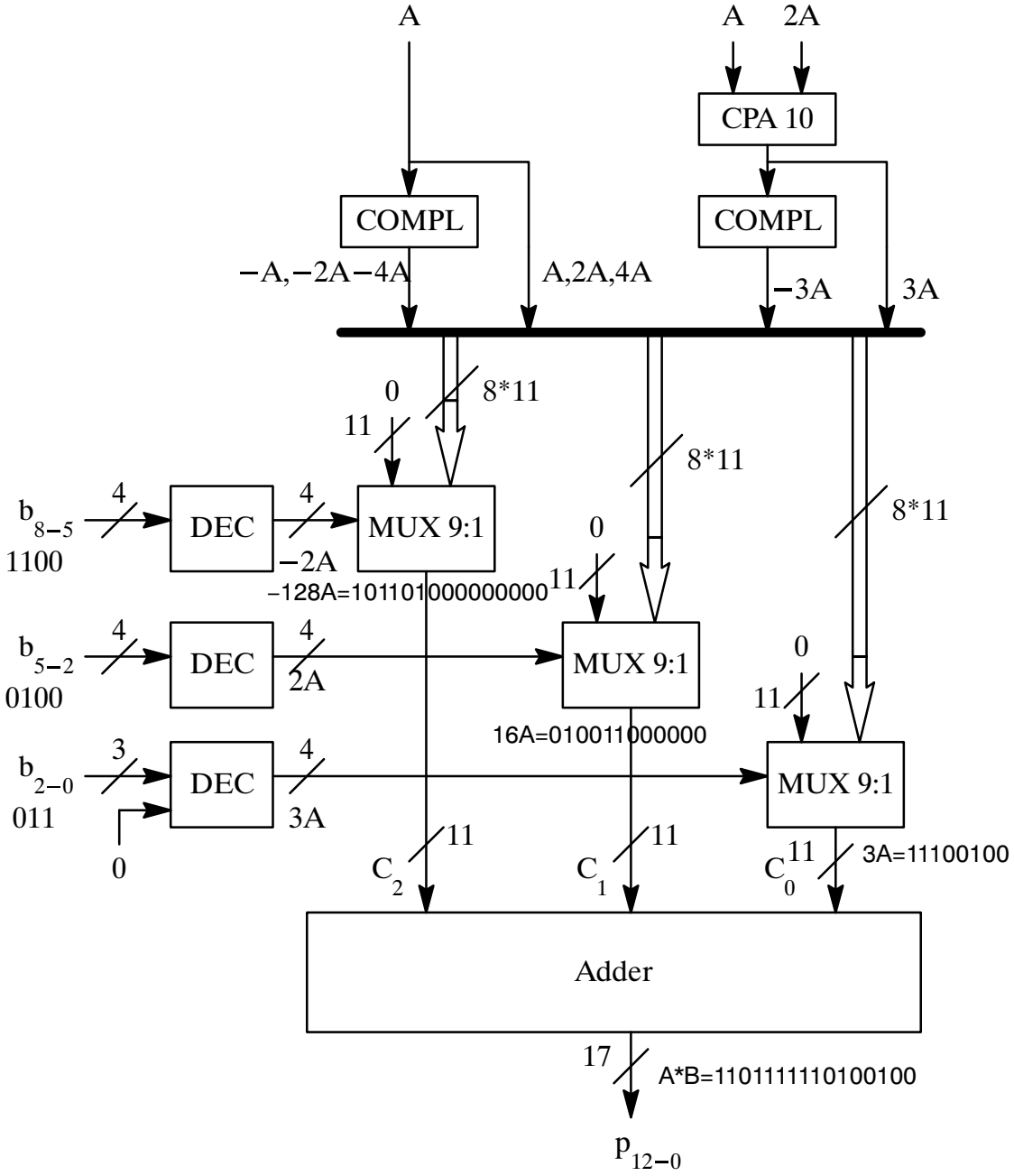
$$k \gtrsim \left\lceil \frac{\log n}{\log \frac{7}{3}} + 1 \right\rceil$$

Exercise 3.9

a.

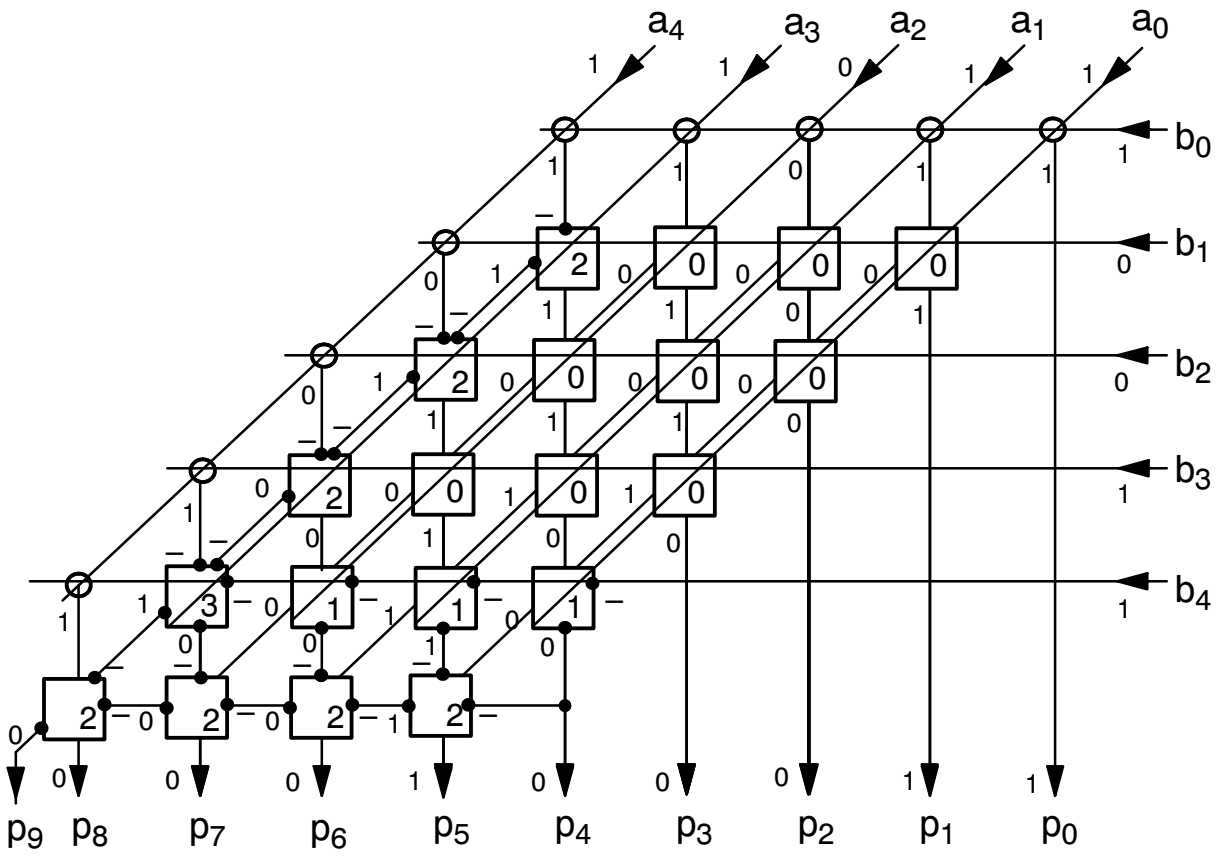


b.

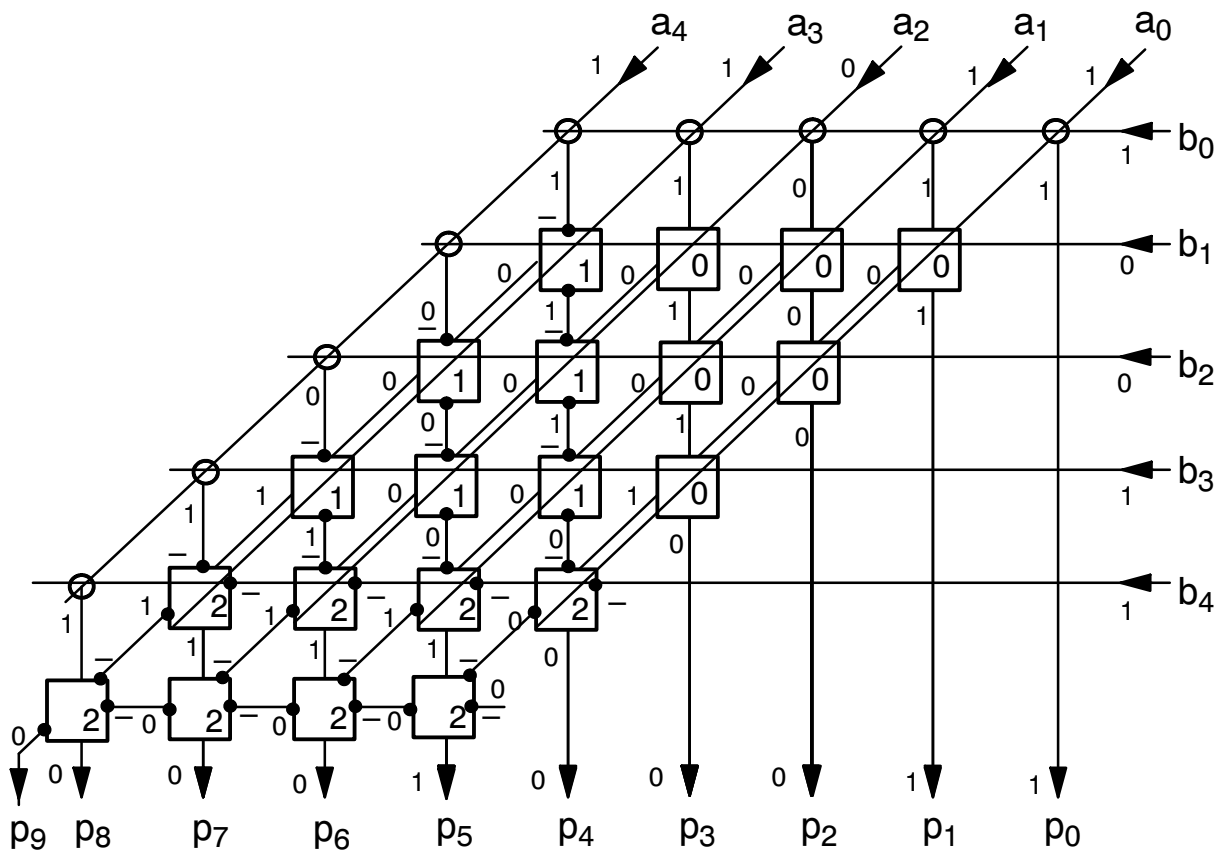

A
A
2A
CPA 10
COMPL
COMPL
−A,−2A−4A
A,2A,4A
−3A
3A
0
8*11
11
8*11
8*11
4
4
b8−5
1100
DEC
MUX 9:1
−2A
−128A=1011010000000000
0
11
4
4
b5−2
0100
DEC
2A
MUX 9:1
0
11
16A=0100110000000
3
4
b2−0
011
DEC
3A
MUX 9:1
0
11
11
11
C2
C1
C0
3A=11100100
Adder
17
A*B=1101111110100100
p12−0

Exercise 3.10

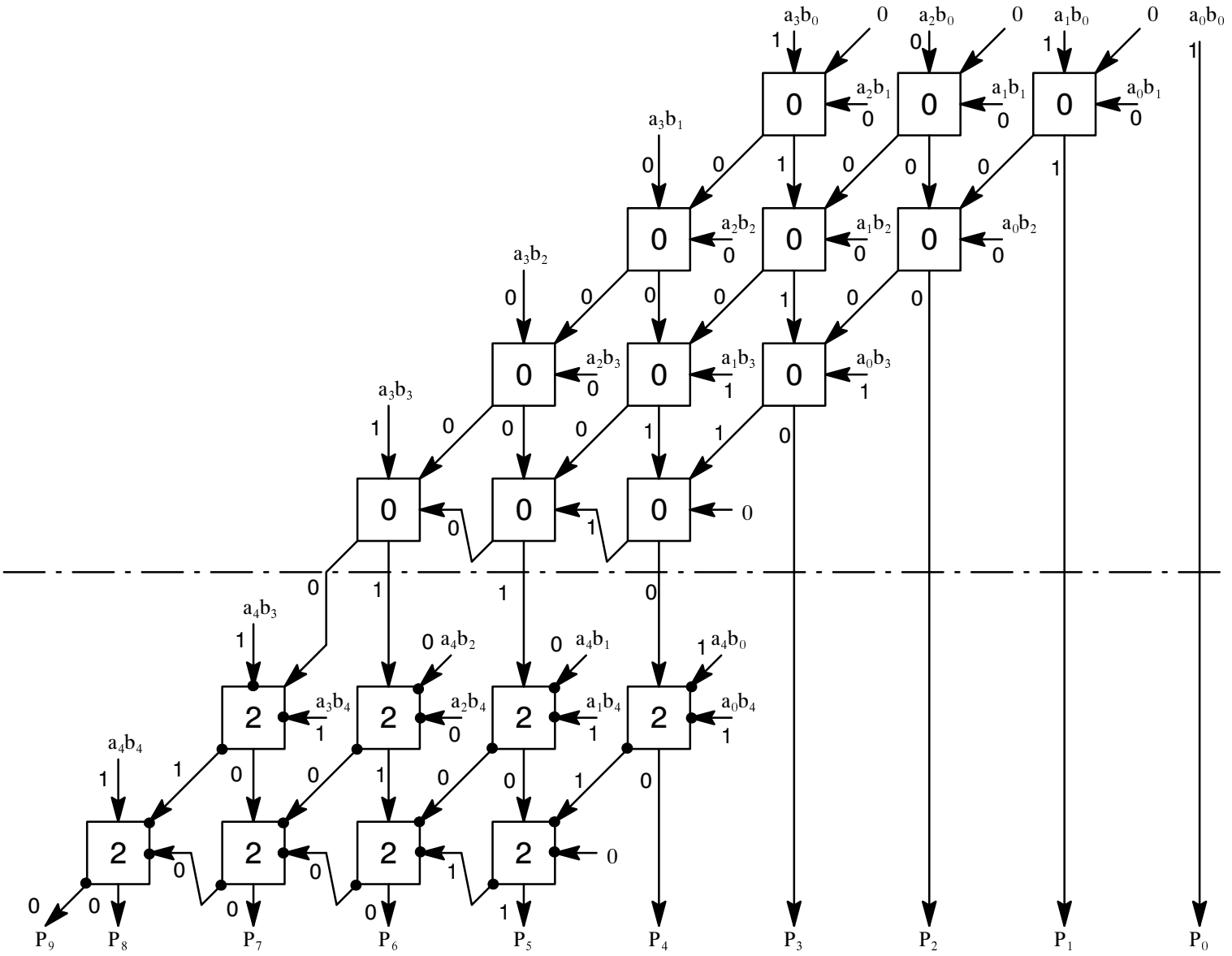
a.



b.



c.

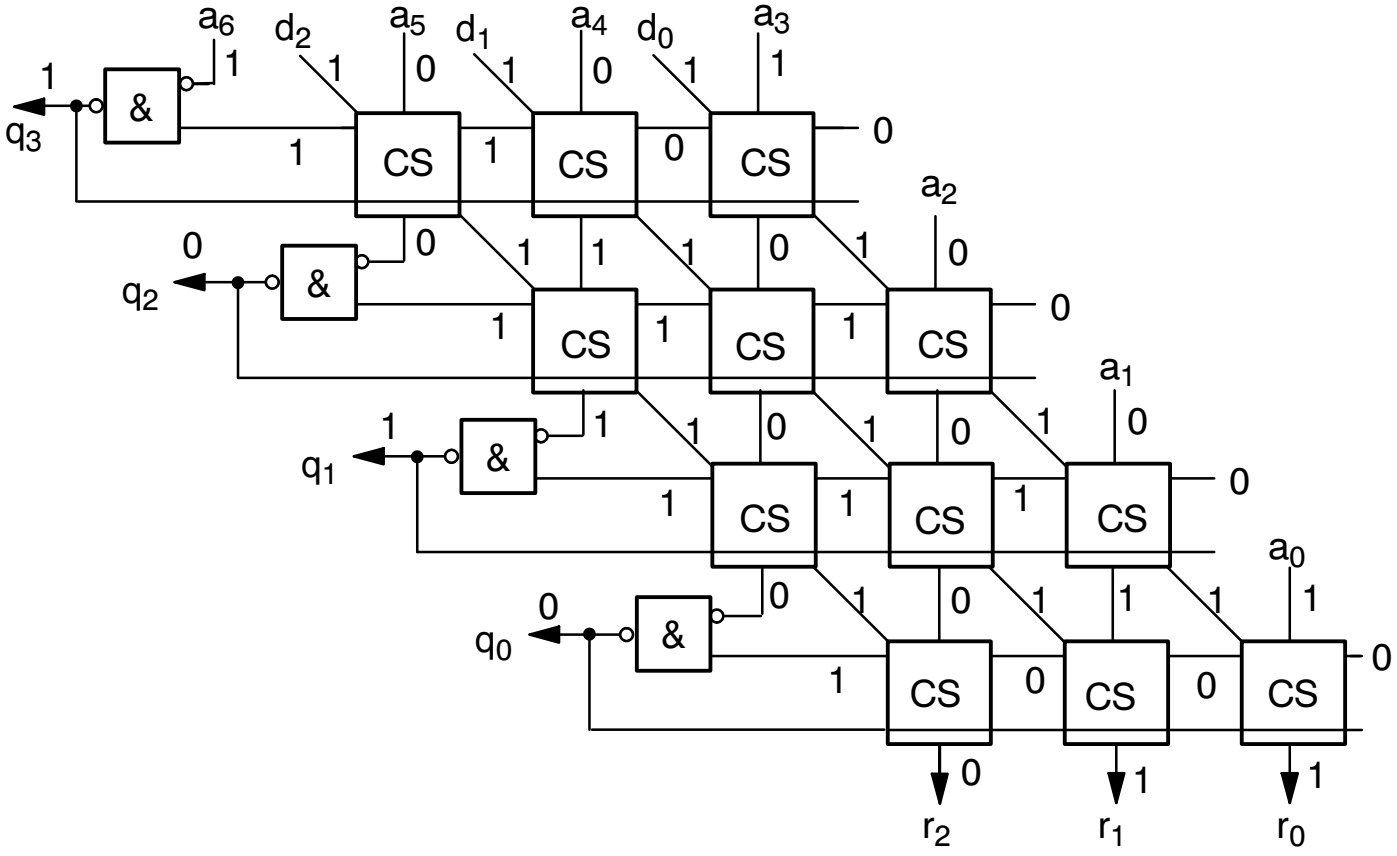

a3b0
a2b0
a1b0
a0b0
a2b1
a1b1
a0b1
a3b1
a2b2
a1b2
a0b2
a3b2
a2b3
a1b3
a0b3
a3b3
a4b3
a4b2
a4b1
a4b0
a3b4
a2b4
a1b4
a0b4
a4b4
P9
P8
P7
P6
P5
P4
P3
P2
P1
P0

Exercise 3.11

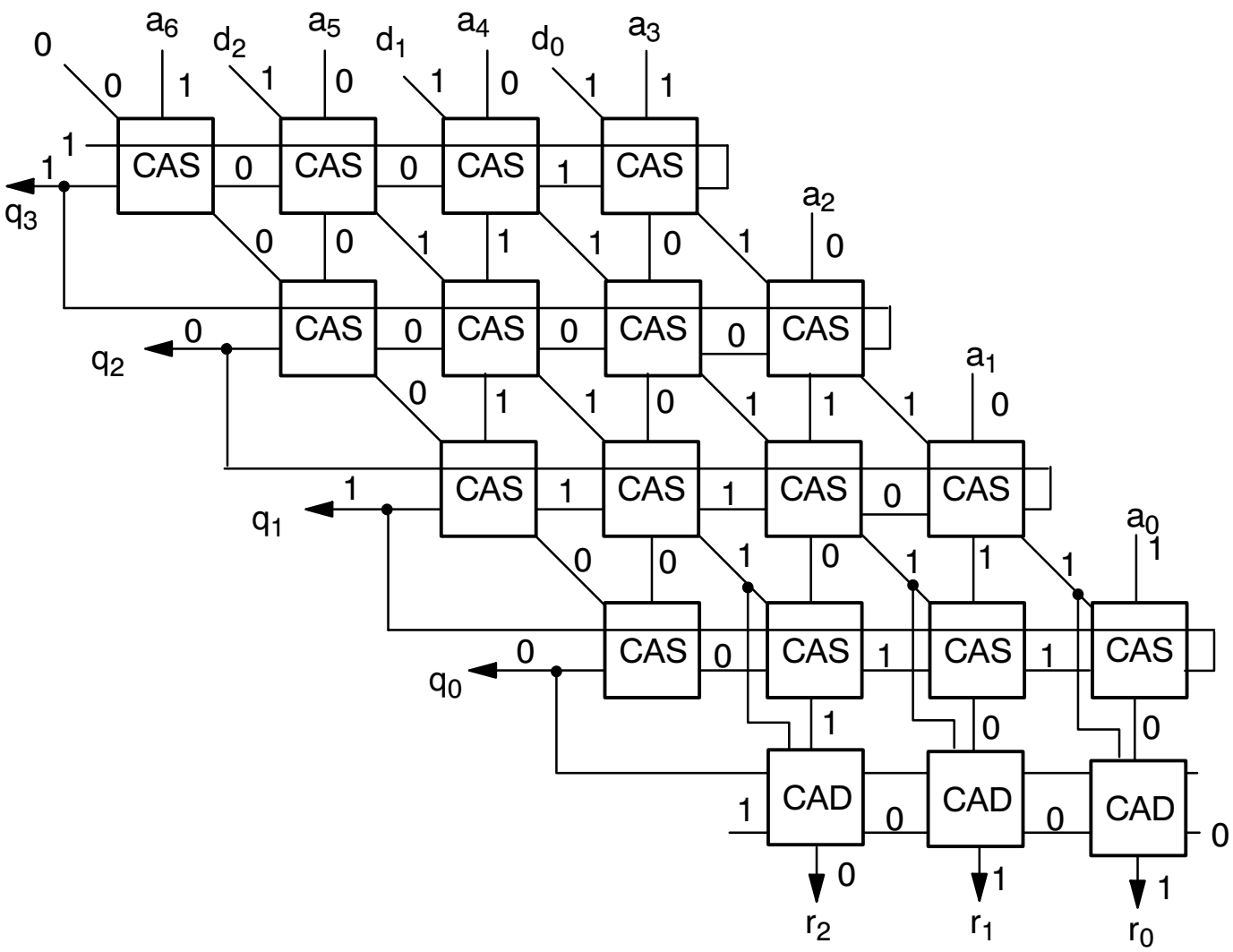
a.

		1	0	0	1	0	0	1:	1	1	1	=	1	0	1	0
–			1	1	1											
				1	0	0										
–				1	1	1										
	(1)	1	1	1	0	1										
R				1	0	0	0									
–					1	1	1									
							1	1								
–						1	1	1								
	(1)	1	1	1	1	1	0	0								
R							1	1								

b.



c.



Exercise 3.12

a. Correction factors k_m:

$m = 1$: Sequence: 0,1,2,3,4,5 $\quad k_m^{-1} = 1.6465$

$m = 0$: Sequence: 1,2,3,4,5,6 $\quad k_m^{-1} = 1$

$m = -1$: Sequence: 1,2,3,4,4,5,6 $\quad k_m^{-1} = 0.82330$

b. Calculation of $\cos(z_0)$ and $\sin(z_0)$

$x_0 = 1,\ y_0 = 0,\ z_0 = z_{0,}\ m = 1,\ z_n \rightarrow 0$

Result:

$x_6 = \cos(z_0) * k^{-1}$

$y_6 = \sin(z_0) * k^{-1}$

i	x_i	y_i	z_i	σ_i	$\text{atan}2^{-i}$	k^{-I}
0	1	0	0.10110	1	.11001	1.41
1	1	1	1.11101	−1	.01111	1.58
2	1.1	0.1	0.01100	1	.01000	1.64
3	1.011	0.111	0.00100	1	.00100	1.64
4	1.01000	1.00001	0.00000	1	.00010	1.65
5	1.00110	1.00011	1.11110	−1	.00001	1.65
Result	1.00111	1.00010	1.11111			

$cos(z_0) = 1.00111_b/1.65 = 0.76$

$sin(z_0) = 1.00010_b/1.65 = 0.64$

c. Multiplication by k

$m = 0,\ y_0 = 0,\ x_0 = in,\ z = k,\ z_n \rightarrow 0,$ Result: y

d. $e^w : m = -1,\ x_0 = 1,\ y_0 = 1,\ z_0 = w,\ z_n \rightarrow 0,$ Result: x or y

$\sqrt{w} : m = -1,\ x_0 = w + .25,\ y_0 = w - .25,\ z_0 = 0,\ y_n \rightarrow 0,$ Result: x