The State of Open Source Processors and Open Source Silicon

Stefan Wallentowitz @ Tensilica Day 2017







Open Source Processors vs. ISAs

• Important difference: ISA vs. Implementation

- Open Instruction Set Architecture (ISA)
 - Define the basic interface between SW and HW
 - "ISAs don't matter, ISAs do matter" (K. Asanovic)
 - Can have proprietary implementations
 - Closed ISA: Patents on parts in the ISA

Benefits of an Open ISA

- Innovation and broader market
- Boost open source ecosystem
 - Availability of hardware
 - Shared tools and software ecosystem
- Reduced costs
- "Real" architecture research and education
- Closed ISAs change with their companies

Popular Open ISAs

- Sparc V8:
 - 32-bit ISA by Sun (1990)
 - Adopted as (now inactive) IEEE 1754-1994
- OpenRISC
 - Started as a student project, first release: 2000
 - Active, but small community

RISC-V: The new star open ISA

- Started in 2010, UCB Aspire Lab
- Based on standard RISC principles

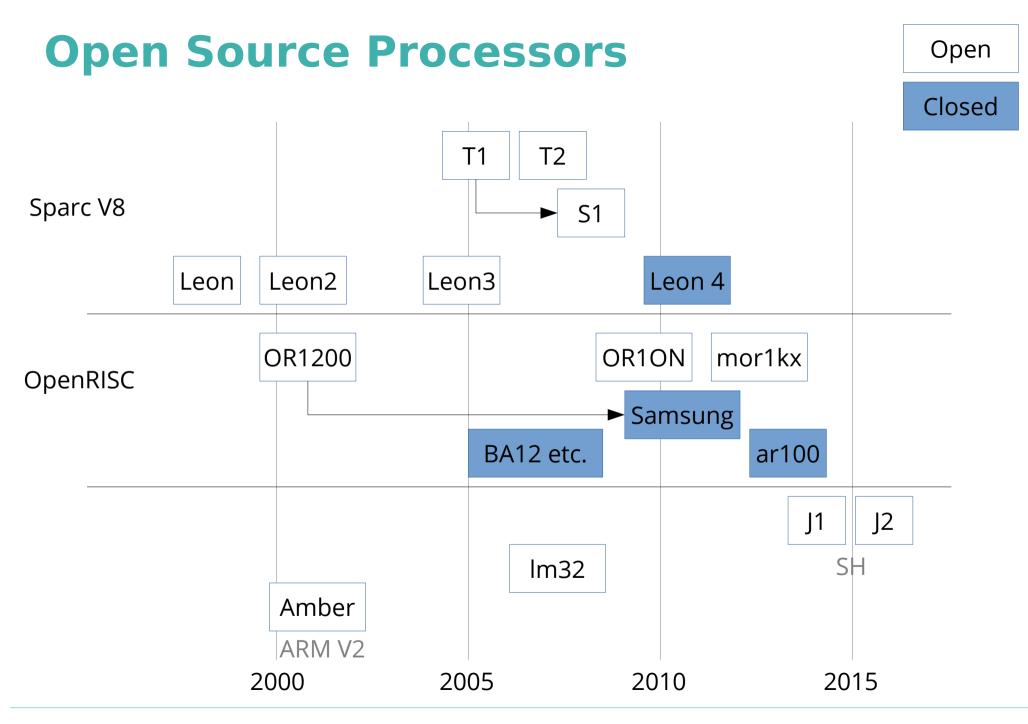


- Integral design concept: custom extensions
- RISC-V Foundation governs the ISA
 - Many industry members
 - A lot of traction



Take me to the open processors!

Chuck Coker via Flickr, CC BY 2.0 https://www.flickr.com/photos/caveman_92223/4016133284/

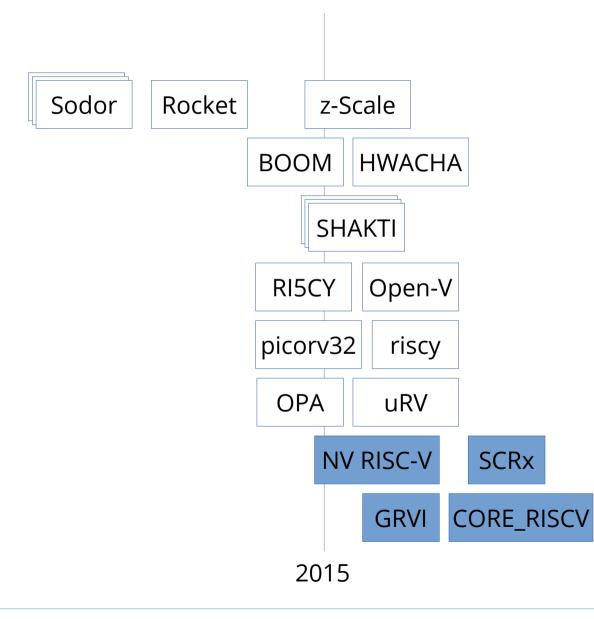


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RISC-V Processors

Open

Closed



LowRISC: An open RISC-V SoC

- Not-for-profit, since 2014
- "Linux of the Hardware World"



- Goal: Produce entirely open SoC, high-quality, secure base for derived works
- Features:
 - Tagged memory
 - Minion cores
- Three releases so far, next in March
- Other activities: RISC-V LLVM

Free and Open Source Silicon

- Hardware was open in the beginning, but
 - Dense integration into single chips
 - It has become a critical, expensive venture
- Uprising of "Open Source Digital Design"
 - First significant wave with opencores.org
 - FPGAs are probably the key enabler
 - Recently: many open source hardware projects
- But: Development of open source "IP" still in its very beginning, learn from software and makers

When I think of hardware development...

	X	HDS Setup Assistant Wizard 🗸 🔨 🗙
→ HDS Setup Assistant Wizard Version Management → Language ↓ Verling 2005 (Graphics) ↓ Verling 2005 (Graphics) ◇ Yes ↓ Vype Of Design ◇ Yes ⊕ - FPGA ◇ No ⊖ MODEL_SIM Choose which Version Management interface ♥ Synthesis ○ Synthesis ○ Other Flows Version Management Ir Project Setup ○ UART (VERILOG 2001) ○ Design Library Version Management Version Management Synthesis ○ Back Next >	 Language Verilog 2005 (Graphics) VHDL 2008 (Text VHDL) SystemVerilog (Text Verilog) Type Of Design FPGA Xilinx Simulator MODEL_SIM Synthesis SYNPLIFY Other Flows HDL Generation from C/C++ I/O Designer Project Setup UART (VERILOG 2001) Design Library 	o you want to enable Version Yes No noose which Version Management interface ersion Management Ir <u>RCS (provided with HDS)</u> ClearCase VSS SS CVS (provided with HDS) SVN ₩

Screenshot from Mentor Graphics HDL Designer v2016.1 (own work)

35 m days



How can we improve that, especially for FOSSi?

Photo by VFS Digital Design via Flickr, CC-BY 2.0 https://www.flickr.com/photos/vfsdigitaldesign/5396691102

Permit

0.25

Brody

Writer.

Script

FOSSi Foundation

- Non-profit organization
 - Started from OpenRISC community



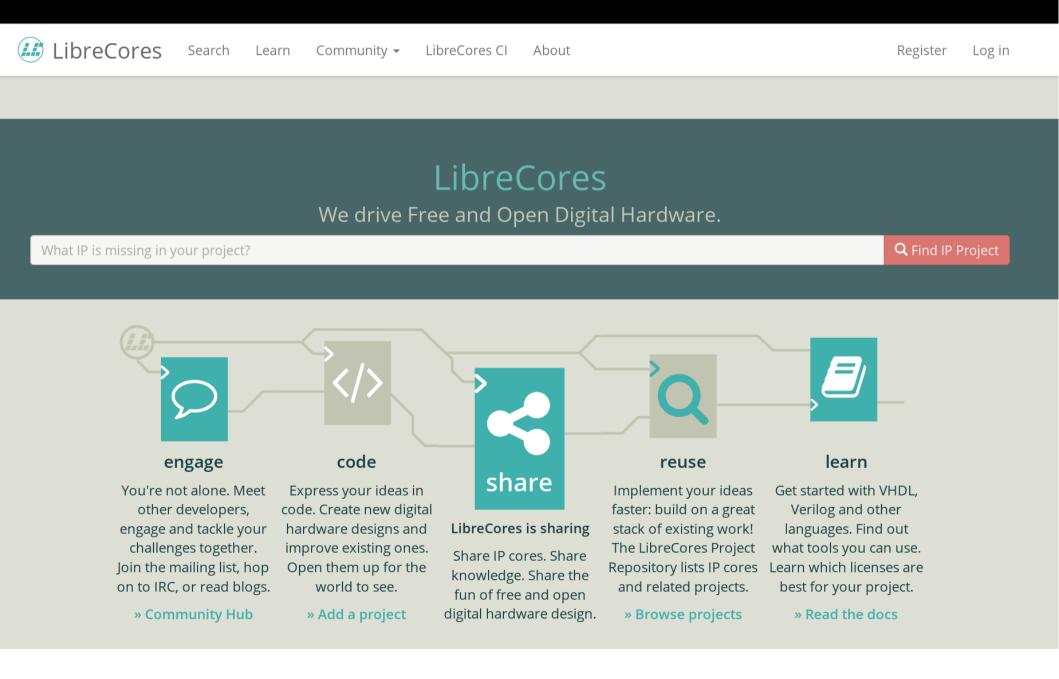
- Not happy with stagnation of opencores.org
- Goal: Advance "Free and Open Source Silicon"
- Three main activities of FOSSi
 - Community hub LibreCores.org
 - Licensing
 - Community Involvement, Conference

We need more collaboration!

BECYCLE REDUCE

Kevin Dooley via Flickr, CC BY 2.0 https://www.flickr.com/photos/pagedooley/8435953365

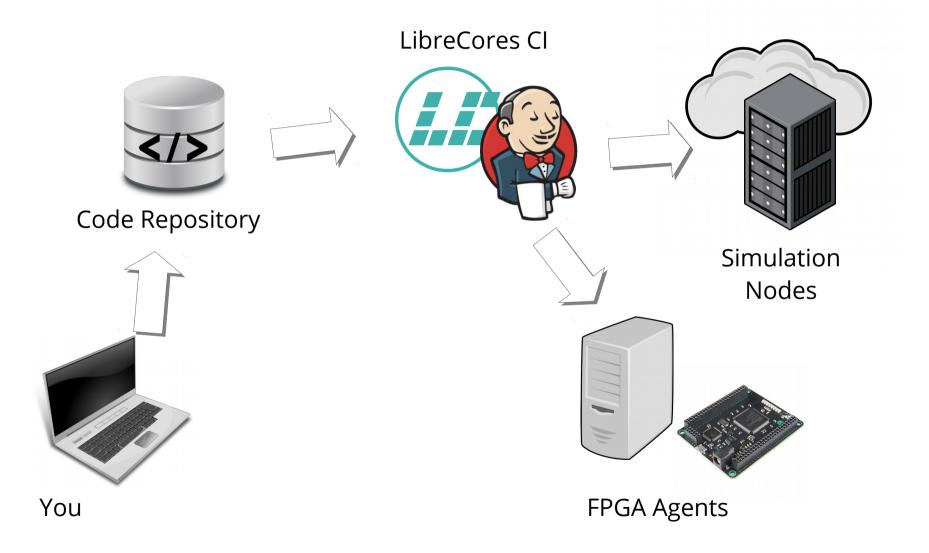
Say Hello to LibreCores!



LibreCores Status & Plans

- Heavy development, currently basic features
 - We don't host code, others do that better
 - Present metadata around your core
- Focus is on trust, collaboration, integration
- Plans for 2017:
 - Quality Metrics (machine-/community-generated)
 - API-Integration with package managers
 - Extensive tutorials and best-practices
 (How to host, publish, license, etc.)

LibreCores Continuous Integration



FPGA board: Sparkfun CC BY-NC-SA 3.0

The inevitable topic

verkeorg via Flickr, CC BY-SA 2.0 https://www.flickr.com/photos/verkeorg/25102323896/

Licensing

- Area of most confusion
- FOSSi Foundation licensing committee
- Publish articles about license choices
- Roadmap 2017: Three recommendations
 - Permissive license: Solderpad License
 - Weak copyleft: GPL+?, OHDL
 - Strong copyleft: GPL+?, CERN OHL

Community Events

- Upcoming: Open Silicon and RISC-V
 - Munich, 23 March, 2017
 - Krste Asanovic, UC Berkeley: RISC-V
 - Rob Mullins, Alex Bradbury, Uni Cambridge: lowRISC
 - Me: FOSSi Foundation
- Highlight: Our annual conference: ORCONF
 - Started as OpenRISC meeting in 2012
 - Open source digital designs and ecosystem, open source EDA
 - Cambridge 2013 (25 people), Munich 2014 (35), Geneva 2015 (90 people), Bologna 2016 (120 people)

Isn't that a picturesque place?

Rochdale Canal at Hebden Bridge. Poliphilo via Wikimedia Commons, CCO

United Kingdom

Rogaland

Vest-Agder

ORConf 2017

September 8 – 10, 2017

www.orconf.org

Edinburgh

Glasgow



Part of Wuthering Bytes Festival

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Düsseldorf

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rugge

Belgie Belgique

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let's talk!





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