

The State of Open Source Processors and Open Source Silicon

Stefan Wallentowitz @ Tensilica Day 2017



LibreCores

Free and Open
Digital Hardware



FOSSi
Foundation



Open Source Processors vs. ISAs

- Important difference: ISA vs. Implementation
- Open Instruction Set Architecture (ISA)
 - Define the basic interface between SW and HW
 - “ISAs don’t matter, ISAs do matter” (K. Asanovic)
 - Can have proprietary implementations
 - Closed ISA: Patents on parts in the ISA

Benefits of an Open ISA

- Innovation and broader market
- Boost open source ecosystem
 - Availability of hardware
 - Shared tools and software ecosystem
- Reduced costs
- “Real” architecture research and education
- Closed ISAs change with their companies

Popular Open ISAs

- Sparc V8:
 - 32-bit ISA by Sun (1990)
 - Adopted as (now inactive) IEEE 1754-1994
- OpenRISC
 - Started as a student project, first release: 2000
 - Active, but small community

RISC-V: The new star open ISA



- Started in 2010, UCB Aspire Lab
- Based on standard RISC principles
- Base standard extensions (32, 64, 128 bit)
- Integral design concept: custom extensions
- RISC-V Foundation governs the ISA
 - Many industry members
 - A lot of traction

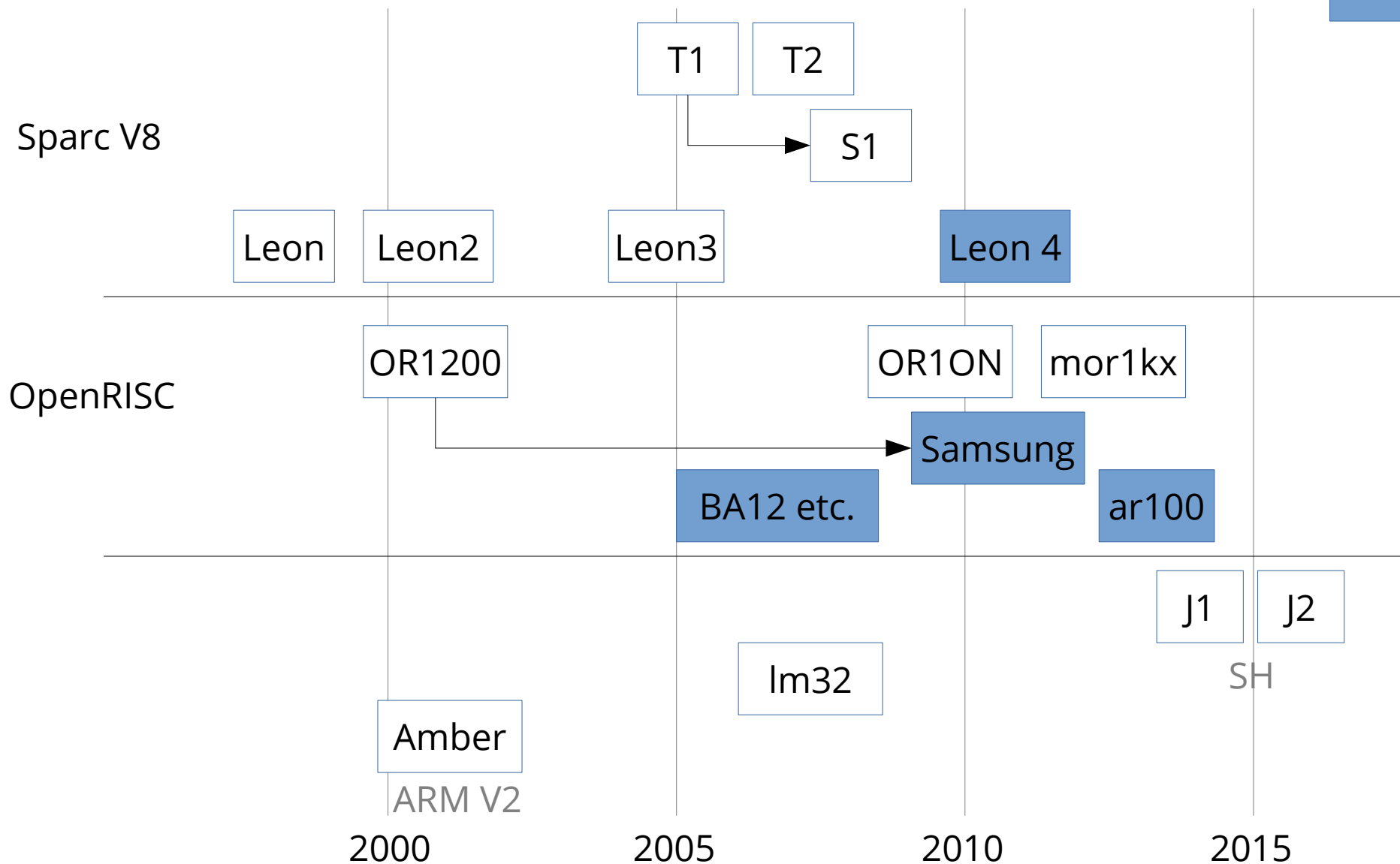


Take me to the open processors!

Open Source Processors

Open

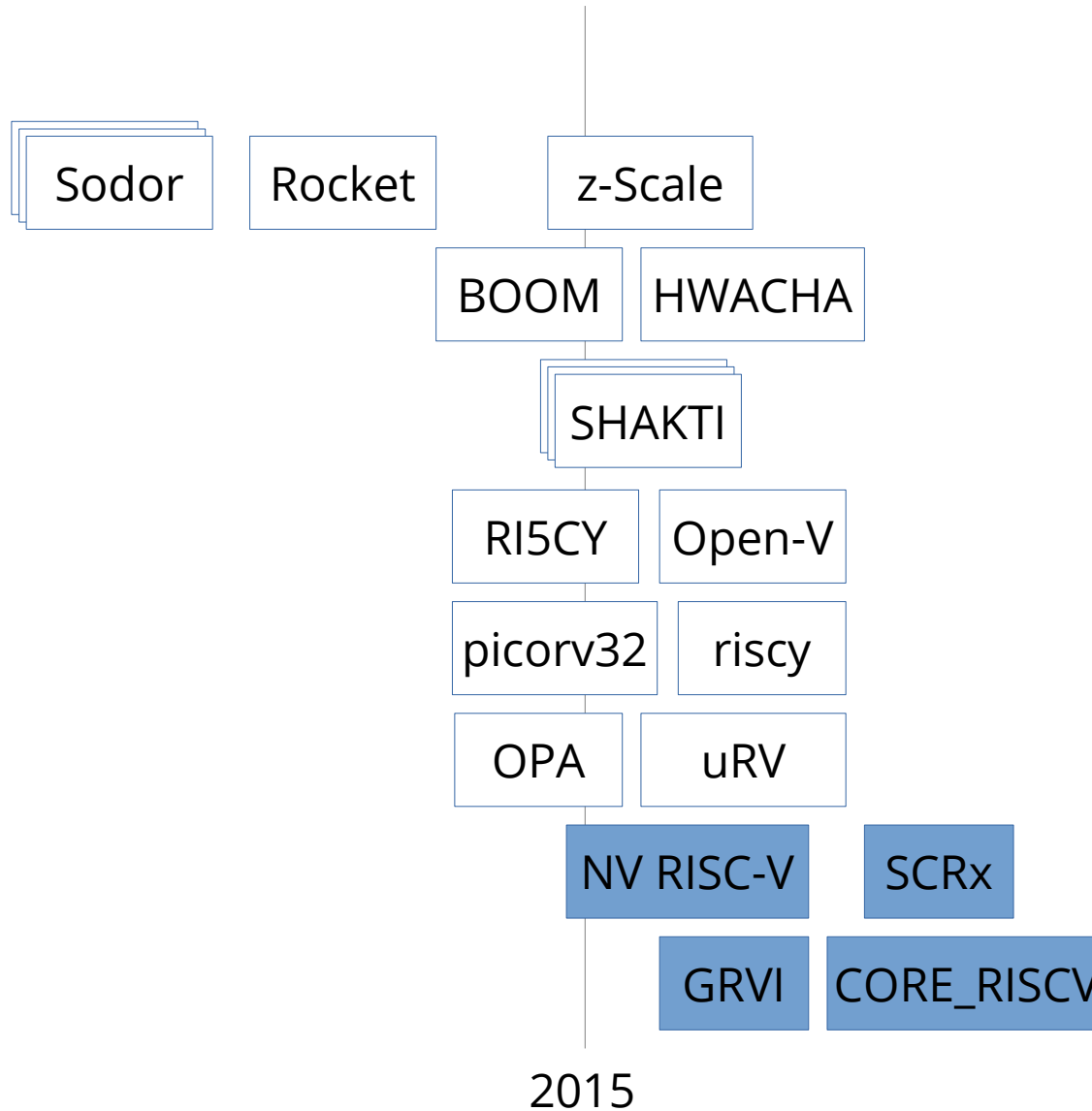
Closed



RISC-V Processors

Open

Closed



LowRISC: An open RISC-V SoC

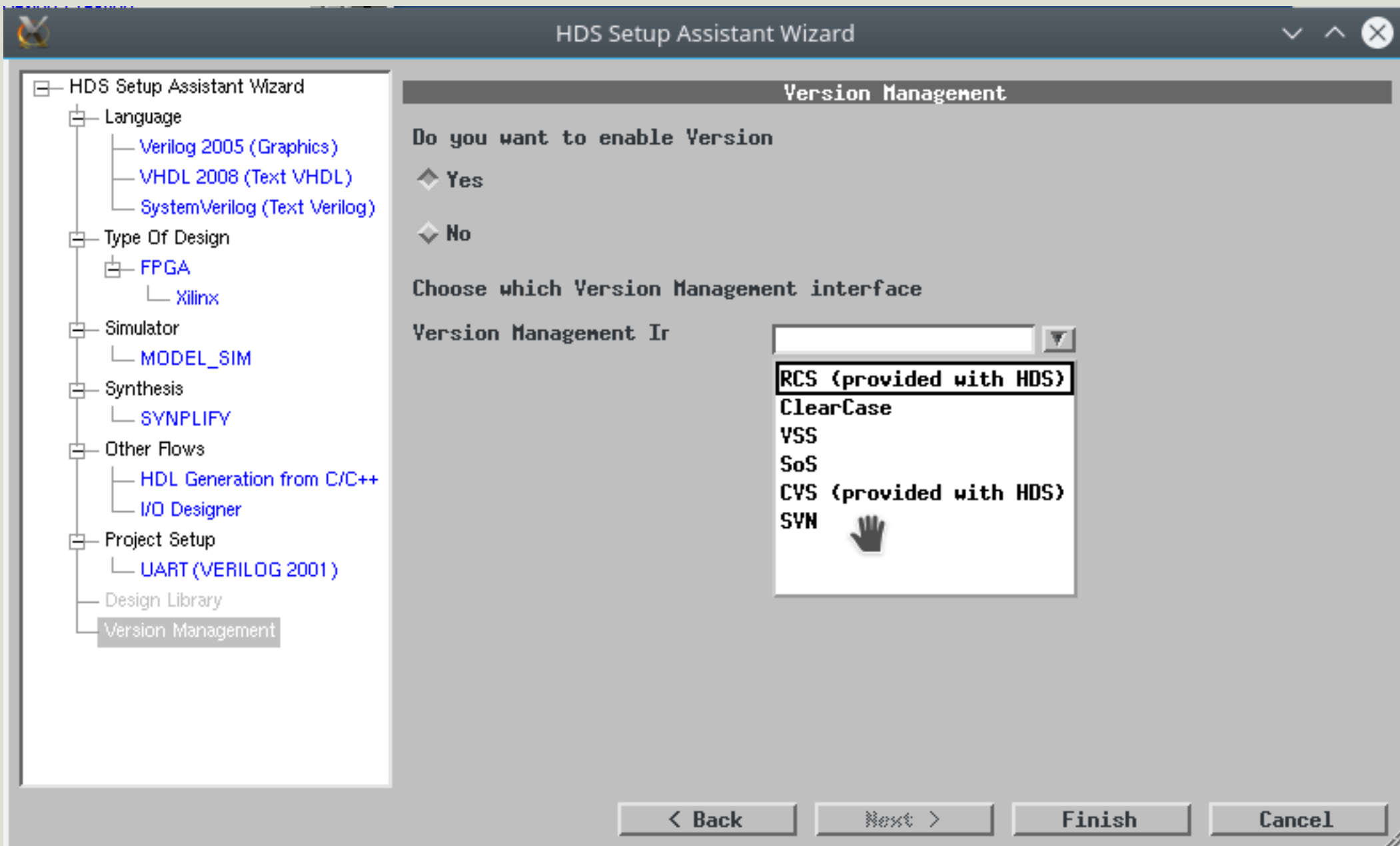
- Not-for-profit, since 2014
- “Linux of the Hardware World”
- Goal: Produce entirely open SoC, high-quality, secure base for derived works
- Features:
 - Tagged memory
 - Minion cores
- Three releases so far, next in March
- Other activities: RISC-V LLVM



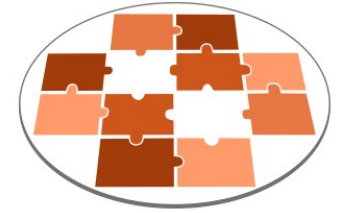
Free and Open Source Silicon

- Hardware was open in the beginning, but
 - Dense integration into single chips
 - It has become a critical, expensive venture
- Uprising of “Open Source Digital Design”
 - First significant wave with opencores.org
 - FPGAs are probably the key enabler
 - Recently: many open source hardware projects
- But: Development of open source “IP” still in its very beginning, learn from software and makers

When I think of hardware development...



FOSSi Foundation



FOSSi
Foundation

- Non-profit organization
 - Started from OpenRISC community
 - Not happy with stagnation of opencores.org
 - Goal: Advance “Free and Open Source Silicon”
- Three main activities of FOSSi
 - Community hub LibreCores.org
 - Licensing
 - Community Involvement, Conference

We need more collaboration!



Say Hello to LibreCores!

LibreCores

We drive Free and Open Digital Hardware.

What IP is missing in your project?

 Find IP Project



You're not alone. Meet other developers, engage and tackle your challenges together. Join the mailing list, hop on to IRC, or read blogs.

» [Community Hub](#)

Express your ideas in code. Create new digital hardware designs and improve existing ones. Open them up for the world to see.

» [Add a project](#)

LibreCores is sharing
Share IP cores. Share knowledge. Share the fun of free and open digital hardware design.

Implement your ideas faster: build on a great stack of existing work! The LibreCores Project Repository lists IP cores and related projects.

» [Browse projects](#)

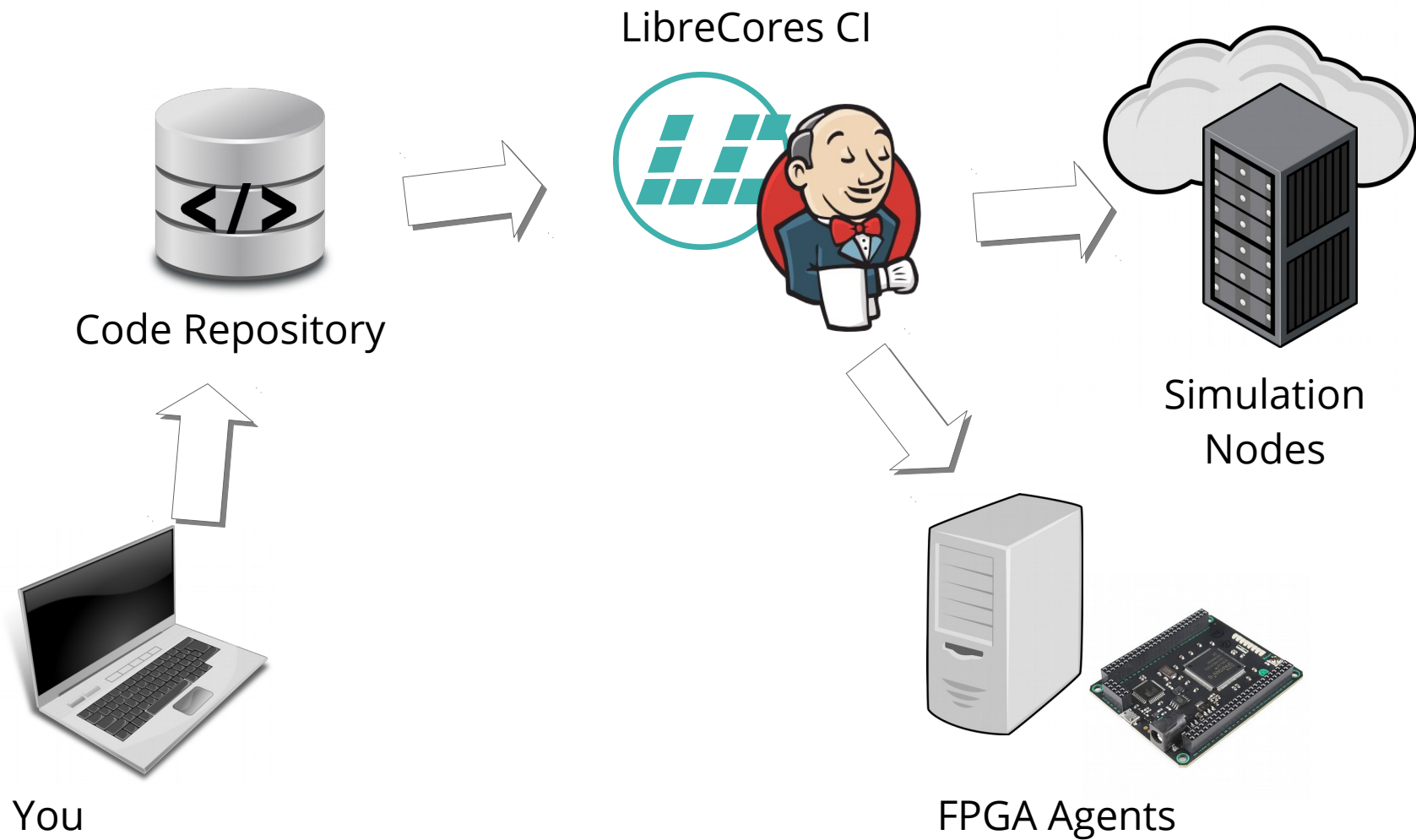
Get started with VHDL, Verilog and other languages. Find out what tools you can use. Learn which licenses are best for your project.

» [Read the docs](#)

LibreCores Status & Plans

- Heavy development, currently basic features
 - We don't host code, others do that better
 - Present metadata around your core
- Focus is on trust, collaboration, integration
- Plans for 2017:
 - Quality Metrics (machine-/community-generated)
 - API-Integration with package managers
 - Extensive tutorials and best-practices
(How to host, publish, license, etc.)

LibreCores Continuous Integration



The inevitable topic



Licensing

- Area of most confusion
- FOSSi Foundation licensing committee
- Publish articles about license choices
- Roadmap 2017: Three recommendations
 - Permissive license: Solderpad License
 - Weak copyleft: GPL+?, OHDL
 - Strong copyleft: GPL+?, CERN OHL

Community Events

- Upcoming: Open Silicon and RISC-V
 - Munich, 23 March, 2017
 - Krste Asanovic, UC Berkeley: RISC-V
 - Rob Mullins, Alex Bradbury, Uni Cambridge: lowRISC
 - Me: FOSSi Foundation
- Highlight: Our annual conference: ORCONF
 - Started as OpenRISC meeting in 2012
 - Open source digital designs and ecosystem, open source EDA
 - Cambridge 2013 (25 people), Munich 2014 (35), Geneva 2015 (90 people), Bologna 2016 (120 people)

Isn't that a picturesque place?



ORConf 2017

September 8 - 10, 2017

www.orconf.org

Hebden Bridge, UK

Part of Wuthering Bytes Festival



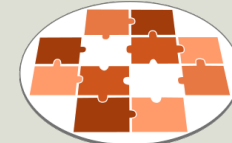
let's talk!



me

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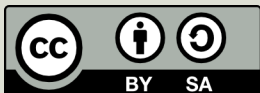
FOSSi Foundation

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#librecores on freenode

Find the slides at:
<https://speakerdeck.com/wallento>



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