TAMPERE UNIVERSITY OF TECHNOLOGY

Co-Design of Programmable Exposed Datapath Processors

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Presentation Outline

Transport Triggered Architectures (TTA):
Exposing the datapath to the programmer

TTA-Based Co-Design Environment (TCE):
A toolset for custom TTA design and programming

Examples of recent TCE design cases

Questions and answers

TRANSPORT TRIGGERED ARCHITECTURES

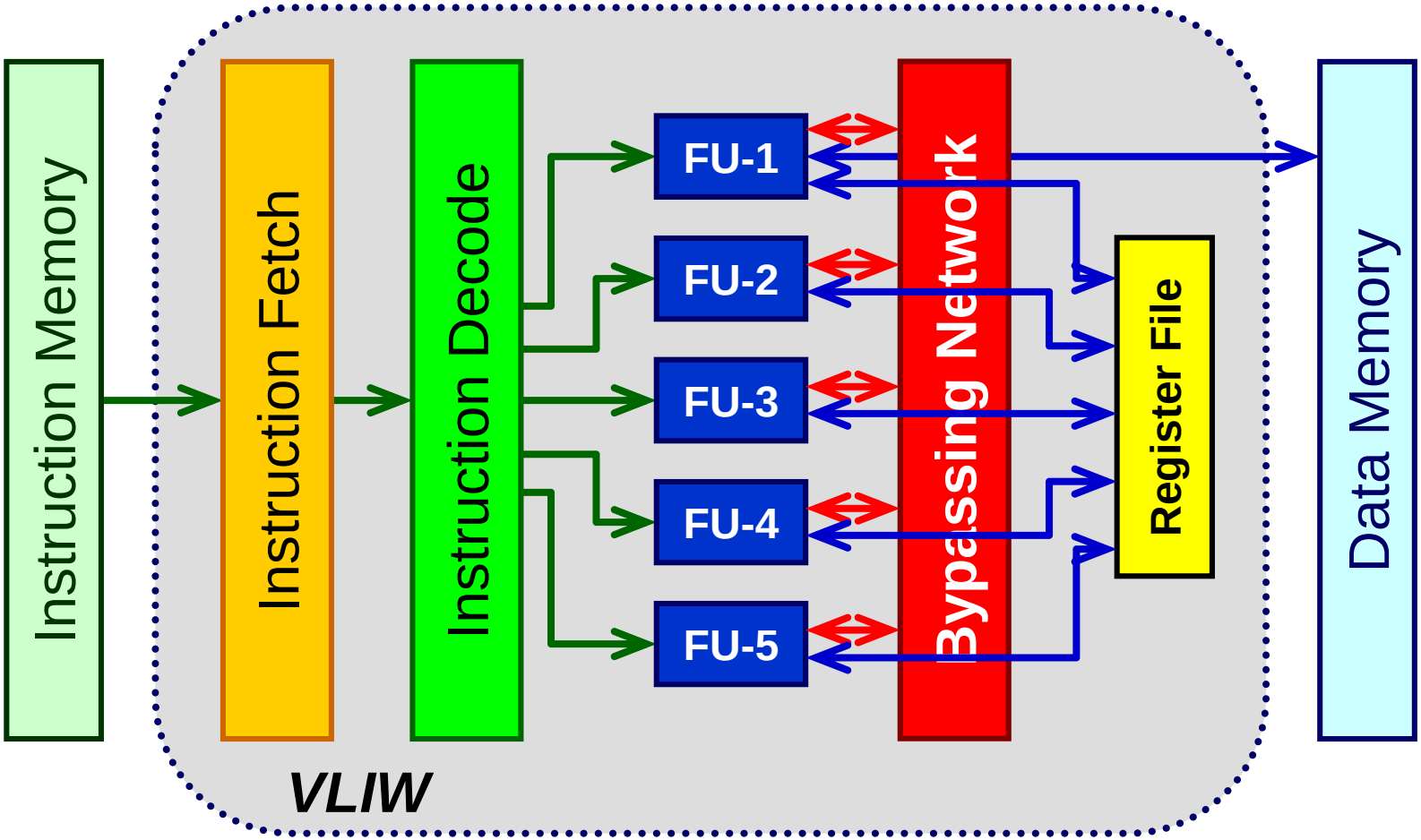
Exposed/Explicit Datapath

- TTA programming model is very fine grained: the programmer controls the datapath operand/result transfers explicitly
- Other academic and commercial architectures with ”exposed datapath” features:
  - FlexCore, Stanford ELM, Static Pipelining, ARM Mali, some AMD GPUs, the Mill/Belt
- The main benefit usually in reduced register file (RF) pressure and simple control hardware
  - Less RF ports needed, less energy wasted on RF accesses
  - Excel in ”number crunching” scenarios (VLIW)

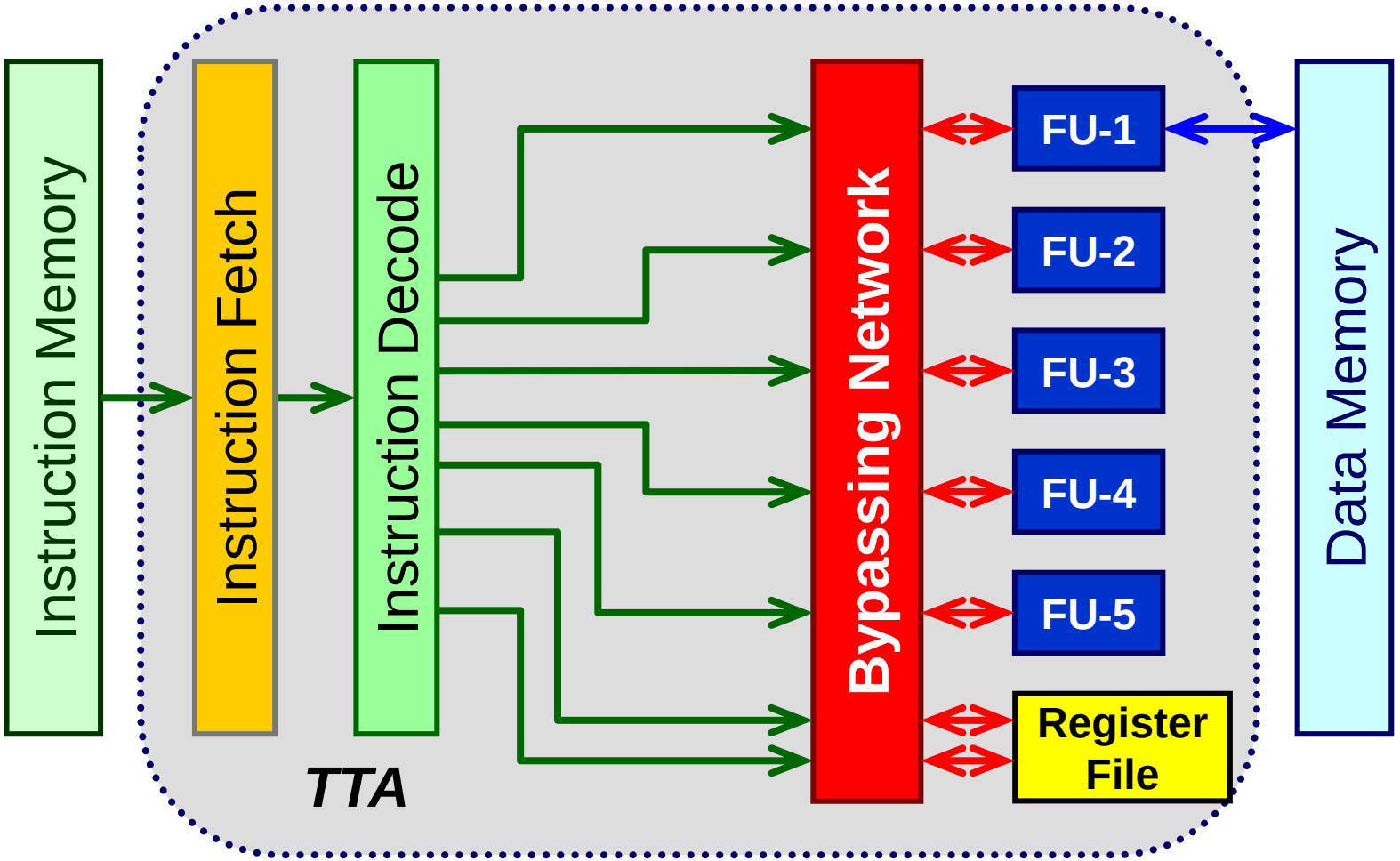
Brief History of Transport Triggered Architectures

- Similar/related ideas already since 1950s
  - English electric DEUCE (1953), GRI Computer GRI 909 (1969), New England Digital's ABLE (1973), Tabak&Lipovski: CMOVE (1976)
- Studied in TU Delft and Eindhoven (since late 1980s)
  - Using TTAs for scalable VLIW designs proposed by Prof. Henk Corporaal et al.
- Ongoing research since early 2000s in our group
  - Builds on Corporaal's TTA research
  - Focus on using TTAs for low power high performance programmable designs, in addition to instruction level parallelism, exploiting also data and thread level parallelism
  - DSP/SDR design case studies

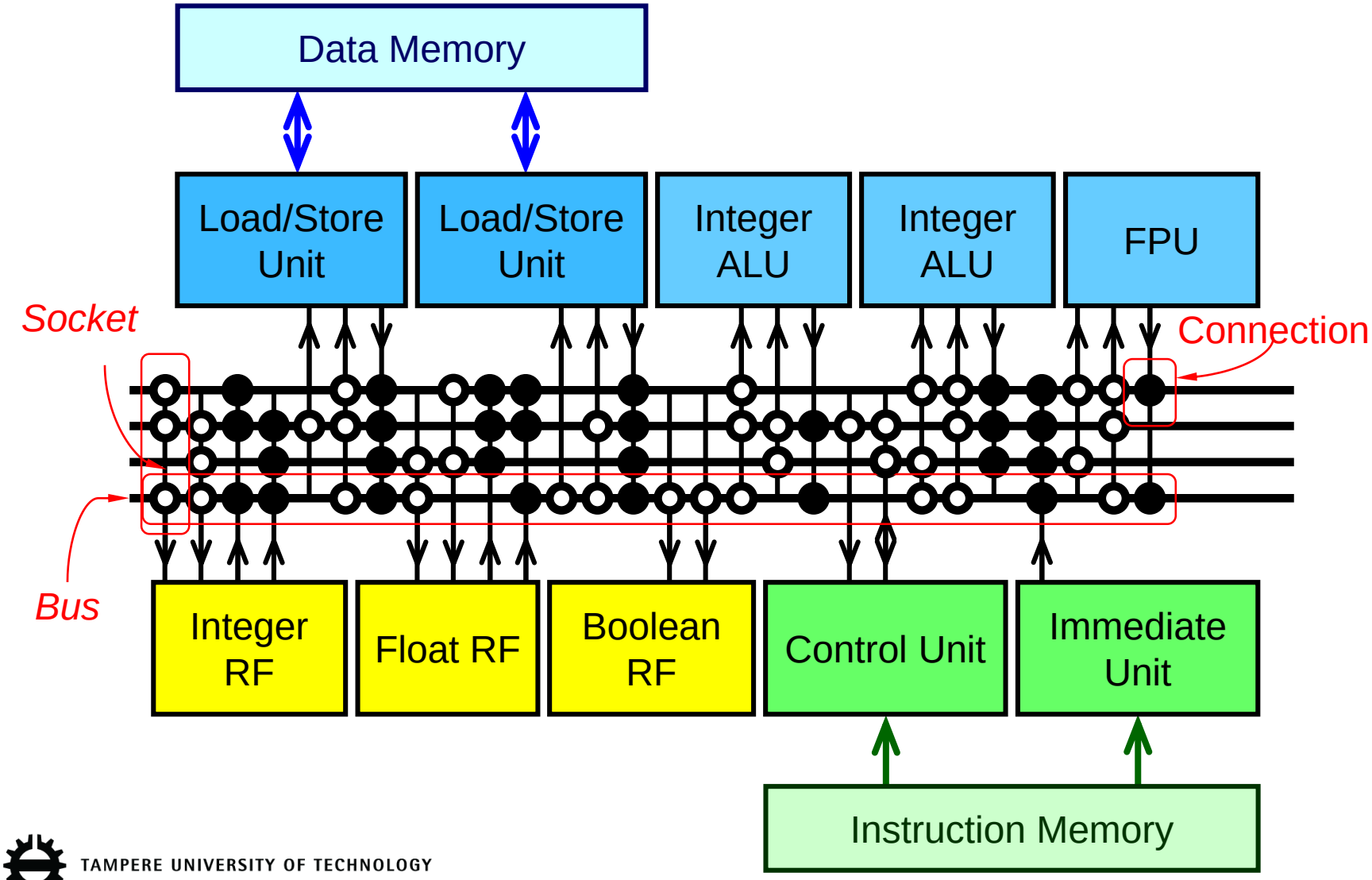
Traditional VLIW



Transport Triggered Architecture



An Example TTA Datapath



Reducing the RF Pressure with TTA Code Optimizations

- Operand/result transport freedom
  - Programmer can control the timing when the RF ports are accessed (often there's "fine grained slack" in the program)
- **Software (register file) bypassing**
  - **The bypass network is controlled by the programmer: can move data directly between FUs without going through RF**
- Dead result move elimination
  - Often all uses of a value can be bypassed: can eliminate the use of the RF for that value completely
- Operand sharing
  - If successive operations in the same FU use the same operand, no need to read it again

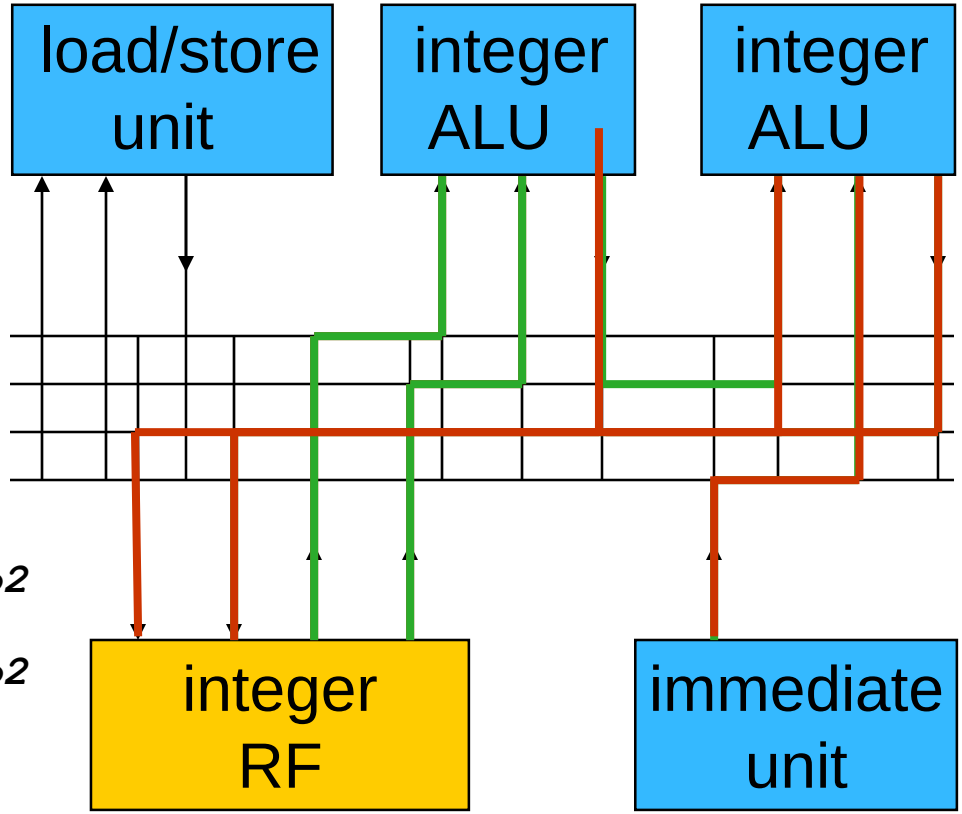
Software Bypassing

Trad. processor

```
add r3,r1,r2

sub r3,r3,99
```

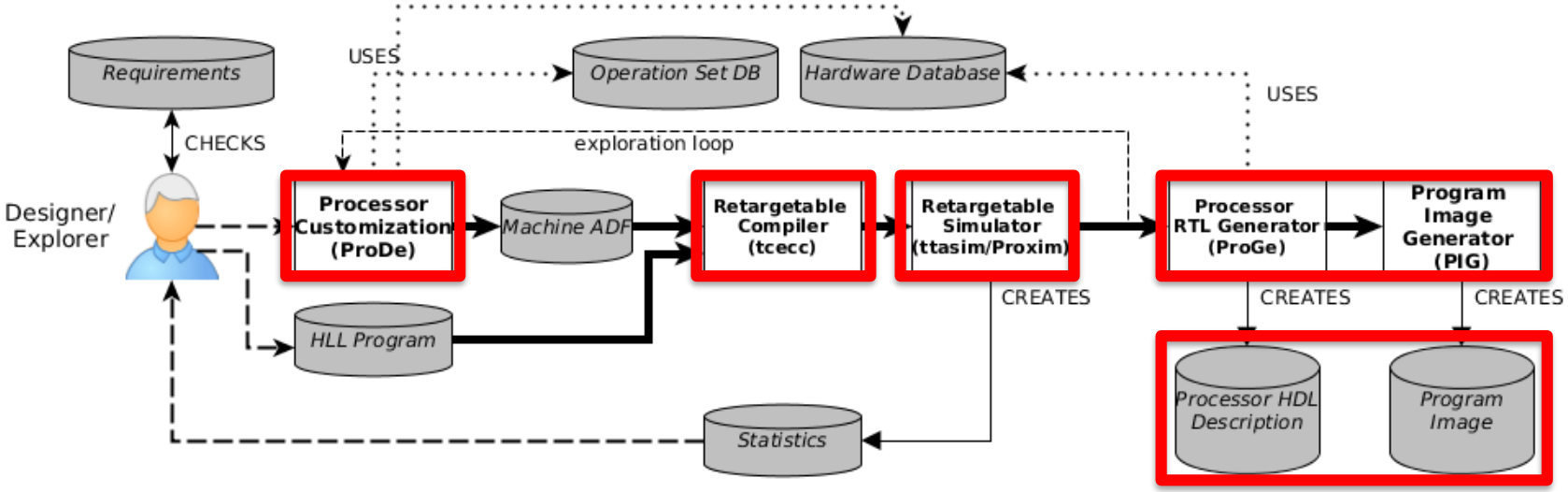
TTA

```
r1 -> add.o1,     r2 -> add.o2

add.r -> sub.o1,  99 -> sub.o2

sub.r -> r3
```



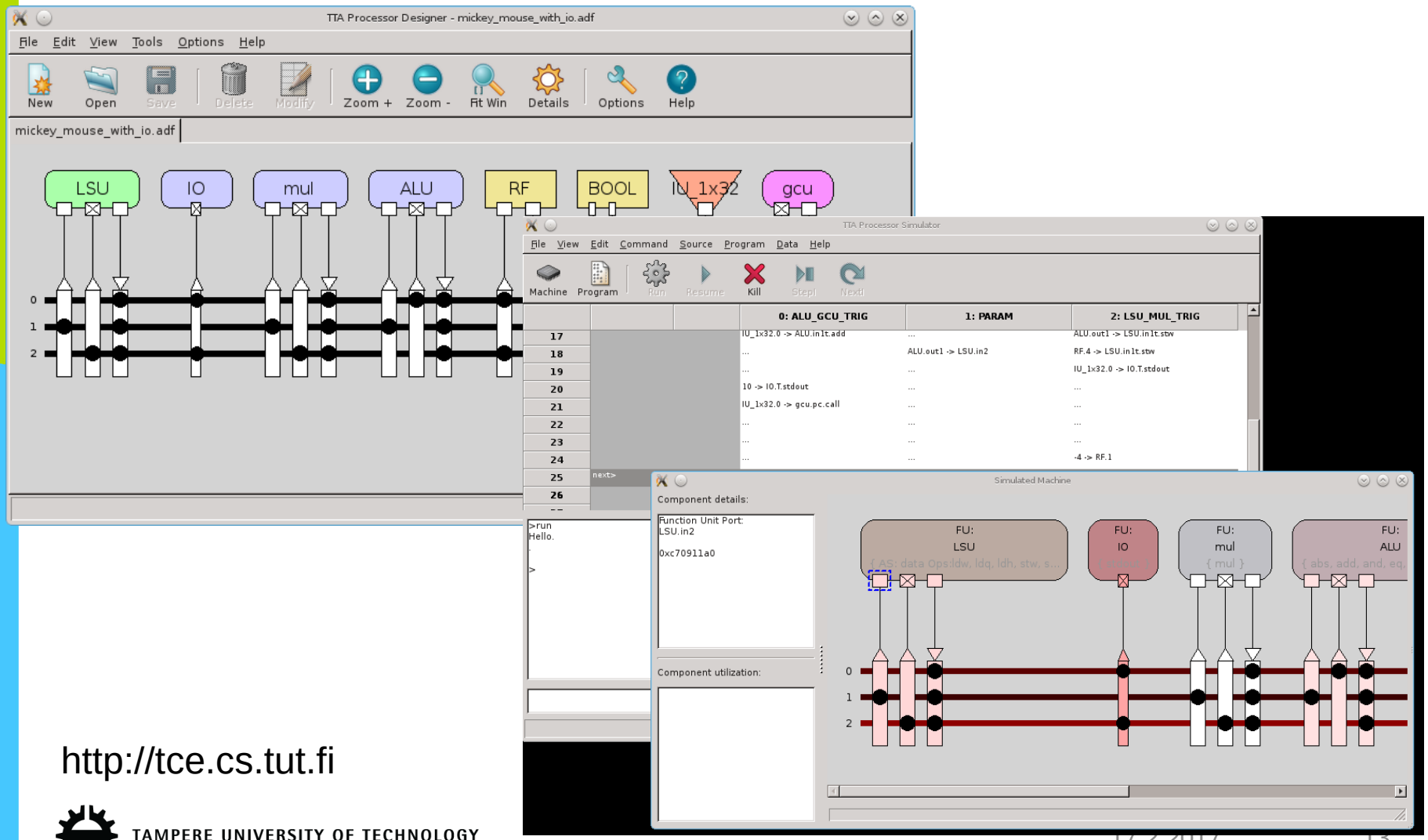
TTA-BASED CO-DESIGN ENVIRONMENT (TCE)

TTA-Based Co-Design Environment (TCE)



- Core tool is tcecc: a retargetable Clang/LLVM-based compiler
- MIT-licensed community version available at http://tce.cs.tut.fi
- Used for several custom processor design cases
  - Video compression, computer vision, software defined radio, audio...
  - Mostly academic case studies, but also commercial cores
- A research platform for customized processors, compilation techniques etc.

TCE Screenshots



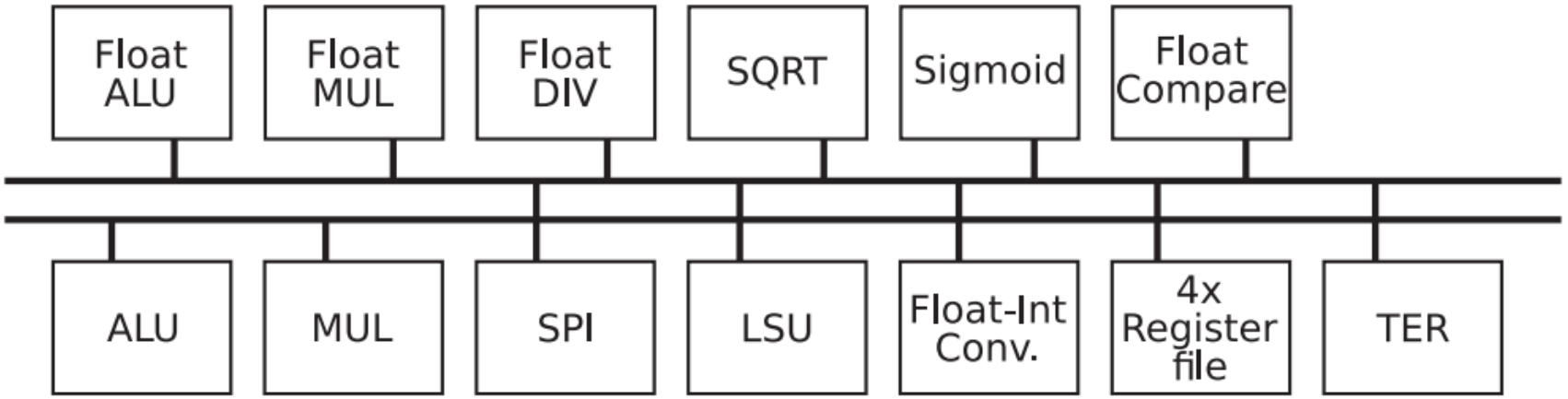
http://tce.cs.tut.fi

EXAMPLES OF TCE DESIGN CASES

Example TCE design case by University of Turku:

A 5.3 pJ/op Approximate TTA VLIW Tailored for Machine Learning

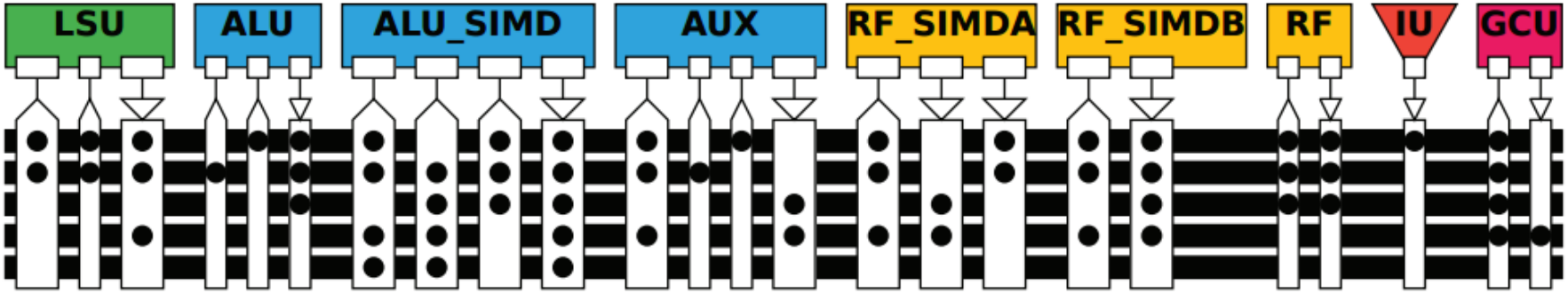
- Minimum energy point 0.35 V near threshold operating voltage for **ultra low power** execution
- Features for approximate computing
  - Detect errors in computation, replace with safe values
- Manufactured on 28 nm FDSOI
- **About 320 µW (incl. memories) on ML workloads**
- Published in Elsevier Microelectronics Journal 61 (2017) 106–113



Example TCEMC design case by Leibniz Universität Hannover:

Customized High Performance Low Power Processor for Binaural Speaker Localization

- Custom DSP targeted to hearing aid devices with support for advanced algorithms:
  - Very low power consumption, high computational performance, small form factor
- 32 x int32 SIMD (1024b) datapath
- Synthesized on 28 nm FDSOI
- 12 mW at 50 MHz, 1V
- 2-split SIMD RF, 1 write port each
  - Only 10.5% of total power thanks to software bypassing and DRE
- Published in 2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)



Summary

- TTA: a modular exposed datapath architecture for data-oriented applications
- TCE: a processor design and programming toolset based on TTA
  - An open source version available
  - Various design experiments done, from high perf. multicores to ultra low power case studies

Thanks!
Questions?

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