



A High-Performance and Ultra Low-Power Processor Architecture for Binaural Hearing Aid Systems. Low-Power Optimization of a VLIW-SIMD ASIP for Hearing Aid Devices

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Motivation for Digital Hearing Aids



- Hearing loss affects about 17% of the adult human population [1]
- Hearing impaired persons often suffer from a loss of temporal and spectral perception
- **Decreased speech intelligibility** in noisy environments
- Digital hearing aids support the hearing aid user in many situations





Requirements for Digital Hearing Aids



- Hearing aid **requirements**:
 - Small and light
 - Long battery life
 - Availability of many algorithms
 - High adaptivity and flexibility
 - Many microphones
 - Small latency

High audio quality







Power Evaluation of Hearing Aid ASIP Optimizations based on the Performance of Algorithms





Evaluation Objective



- **Algorithms**: 3 Beamformer Algorithms
 - Fixed Beamformer
 - Adaptive Filter Beamformer
 - Adaptive Gain Beamformer
- Hardware: 24 optimized ASIP configurations
 - 24-bit up to 64-bit data path width
 - With and without a hardware Co-Processors
 - Register file isolation and dummy registers





- Power
- Area
- Performance



Beamformer Algorithms







Beamformer Algorithms







Beamformer Algorithms







Algorithm Evaluation



- Requirements: Realistic construction of simulated sound fields
- Experimental setup: HRIR database [1]



[1] Kayser, H. et al., 2009

Environment: Anechoic chamber Target source: male speaker Interfering source: moving babble noise

[1] Kayser, H. et al., 2009. Database of multichannel in-ear and behind-the-ear head-related and binaural room impulse responses. EURASIP Journal on Advances in Signal Processing, 2009, p.6.











KAVUAKA VLIW-SIMD ASIP for Hearing Aids [1]

- 2 pipeline stages
- 2 issue slots
- SIMD
- Partitioned register file
- Co-processors
- Multichannel audio interface



[1] Hartig, J.; Gerlach, L.; Payá-Vayá, G.; Blume, H. (2014): Customizing a VLIW-SIMD Application-Specific Instruction-Set Processor for Hearing Aid Devices, IEEE International Workshop on Signal Processing Systems 2014 (SiPS)



Hardware Evaluation



- Evaluation setup:
 - TSMC 40nm Synthesis
 - Netlist simulations of ASIP and co-processors executing the beamformer algorithms
 - Switching activity stored for 700 audio samples, after memories are filled with realistic data
 - Prime Time Signoff Power dynamic power analysis



















Case Study 2: Co-Processor



 $W(n) = \frac{R_{c_1 c_2}(n)}{\hat{R}_{c_1 c_2}(n)}$

- Adaptive Gain Beamformer requires **division** operation:
 - Normalised least mean squares adaptation
- Implementation:
 CORDIC algorithm



ΗW

MVI_32 VxR70, #1 ANDCS_32 VxR70, VxR70, SHIFT_CNT SMVI CONDSEL, #0b0010 // COND_Z MIXL_32 VxR54, VxR53, VxR53 MIXR_32 VxR70, VxR53, VxR53 MVCR_32 VxR70, VxR70 SMVI VxR98, REG_Z_OUT, #0 CONDSEL, #0b0011 // COND_N SUBICS_32 // Kernel equations // x = x - sigma * $2^{(-iteration)} * y$ // y = y + sigma * $2^{(-iteration)} * x$

SW

Performance for 32-bit Fixed Point Division

Processing Cycles	HW-Co-Processor	SW-Library
cycles	113 🔶 4.3	3x ← 489

Gerlach, L.; Nolting, S.; Blume, H.; Payá Vayá, G.; Stolberg, H.; Reuter, C. (2016): A Highly Optimized Arithmetic Software Library and Hardware Co-processor IP for Fixed-Point VLIW-SIMD Processor Architectures, Technology Transfer in Computing Systems (TETRACOM Technology Transfer Project (TTP), 2016)











Case Study 3: Register File Isolation and Dummy Register



Register File (2 x 32 Register)

Bank 0	Bank 1
V0-V31	V0-V31



Case Study 3: Register File Isolation and Dummy Register







Case Study 3: Register File Isolation and Dummy Register











Payá-Vayá, G. et al., 2010. A forwarding-sensitive instruction scheduling approach to reduce register file constraints in VLIW architectures. In Application-specific Systems Architectures and Processors (ASAP), 2010 21st IEEE International Conference on. pp. 151–158.







Case Study 3: Register File Isolation and Dummy Register Power Evaluation



























- Low-Power Optimization of a VLIW-SIMD ASIP for Hearing Aid Devices
 - Objective algorithm evaluations
 - PESQ
 - iSNR
 - STOI
 - Hardware evaluations
 - Dynamic power
 - Area
 - Performance
- With the combination of the hardware and algorithm evaluations, the overall benefit of future hearing aid systems can be increased.