Institute of Microelectronic Systems

Leibniz Universität Hannover

The KAVUAKA Hearing Aid Processor

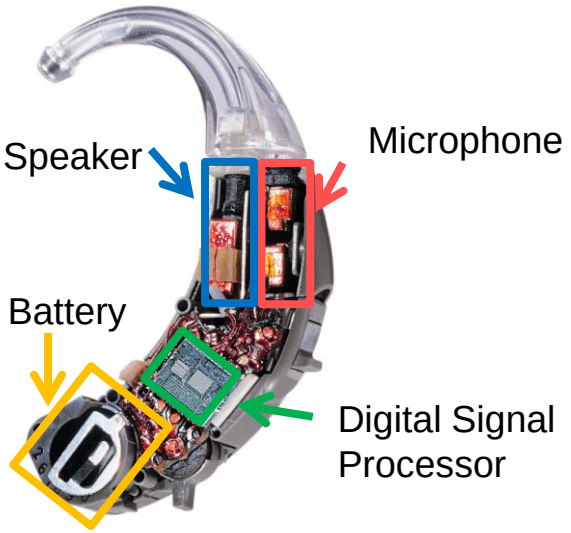
Guillermo Payá-Vayá, Lukas Gerlach, and Holger Blume

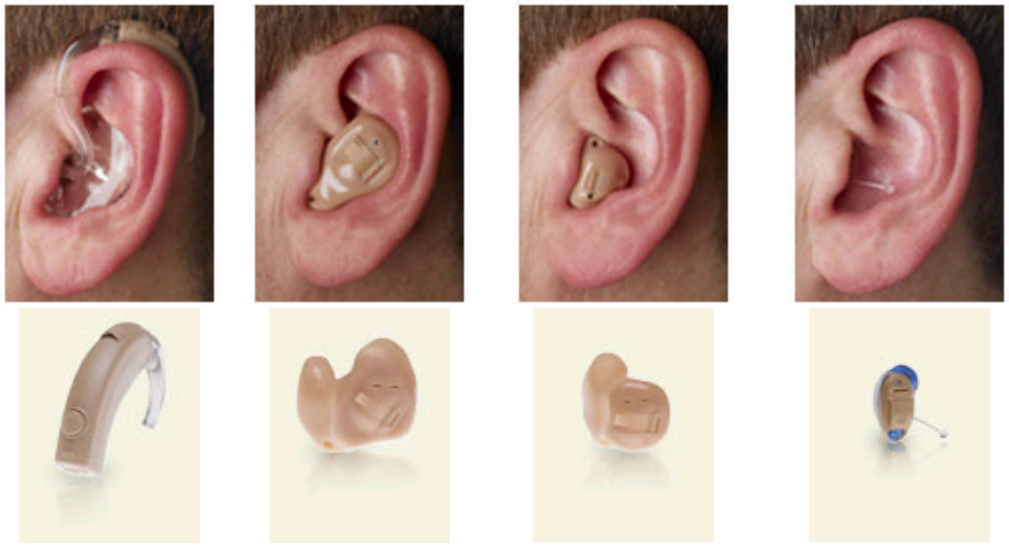
Outline

- Digital Hearing Aid Systems
- The KAVUAKA Hearing Aid Processor
- The KAVUAKA SoC

Digital Hearing Aid Systems

- HA technology requirements
  - Small form factor (higher user acceptance)
  - Low power: *~1 mW* (longer battery lifetime)
  - Low processing delay: *< 10 ms*

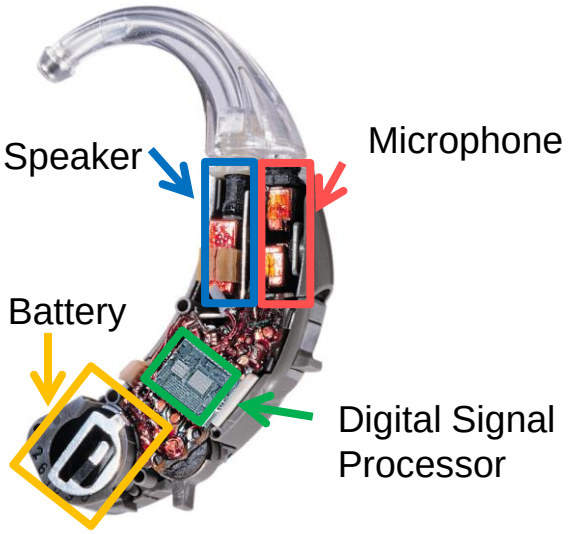


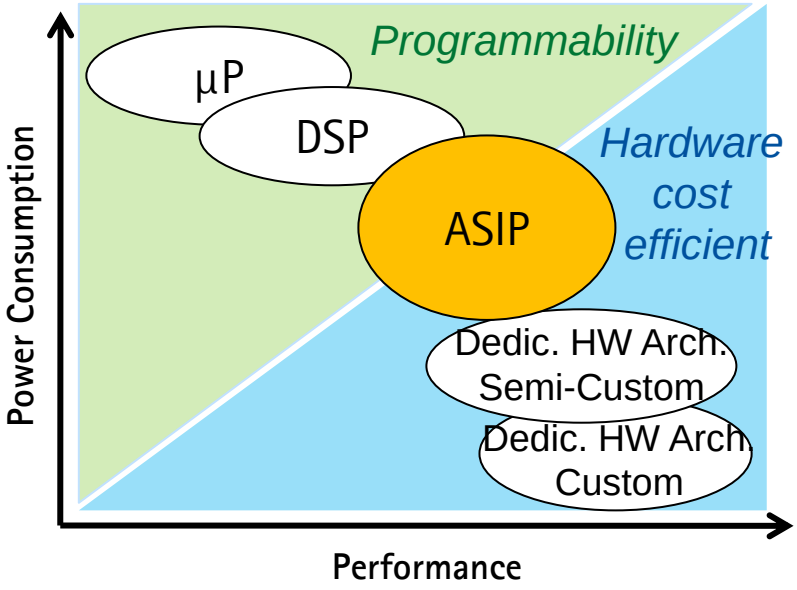


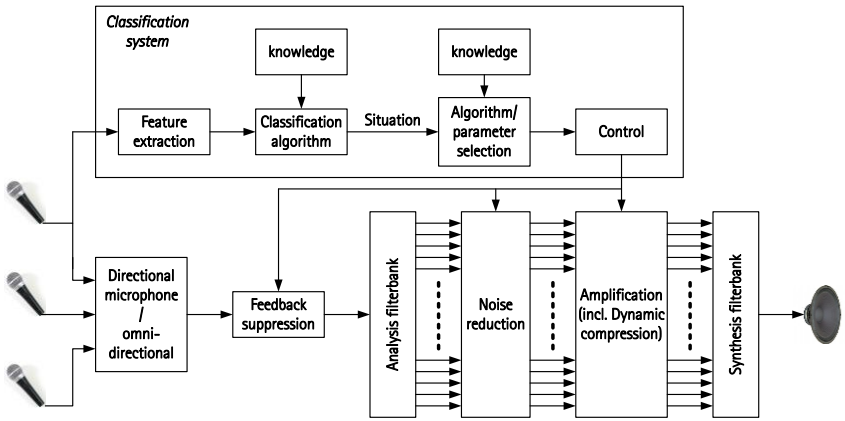
Behind The Ear (BTE) | In-The-Ear (ITE) | In-The-Canal (ITC) | Completely-In-Canal (CIC)

Digital Hearing Aid Systems

- HA technology requirements
  - Small form factor (higher user acceptance)
  - Low power: *~1 mW* (longer battery lifetime)
  - Low processing delay: *< 10 ms*
  - **Programmability / flexibility**

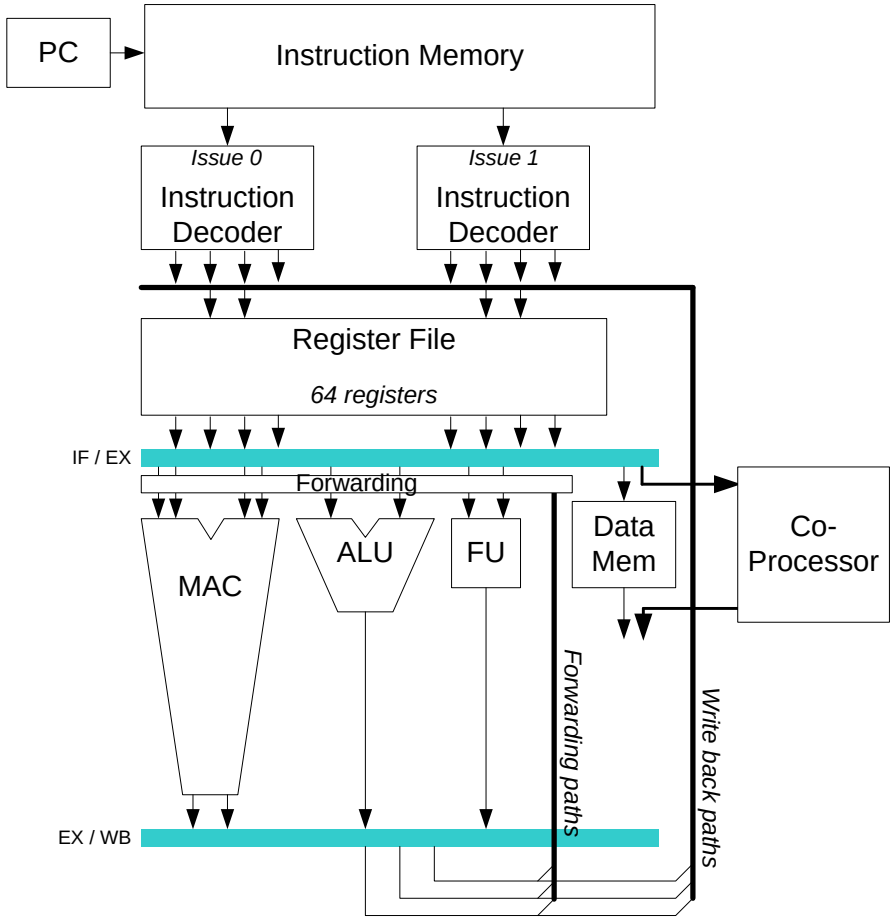






The KAVUAKA Hearing Aid Processor (I)

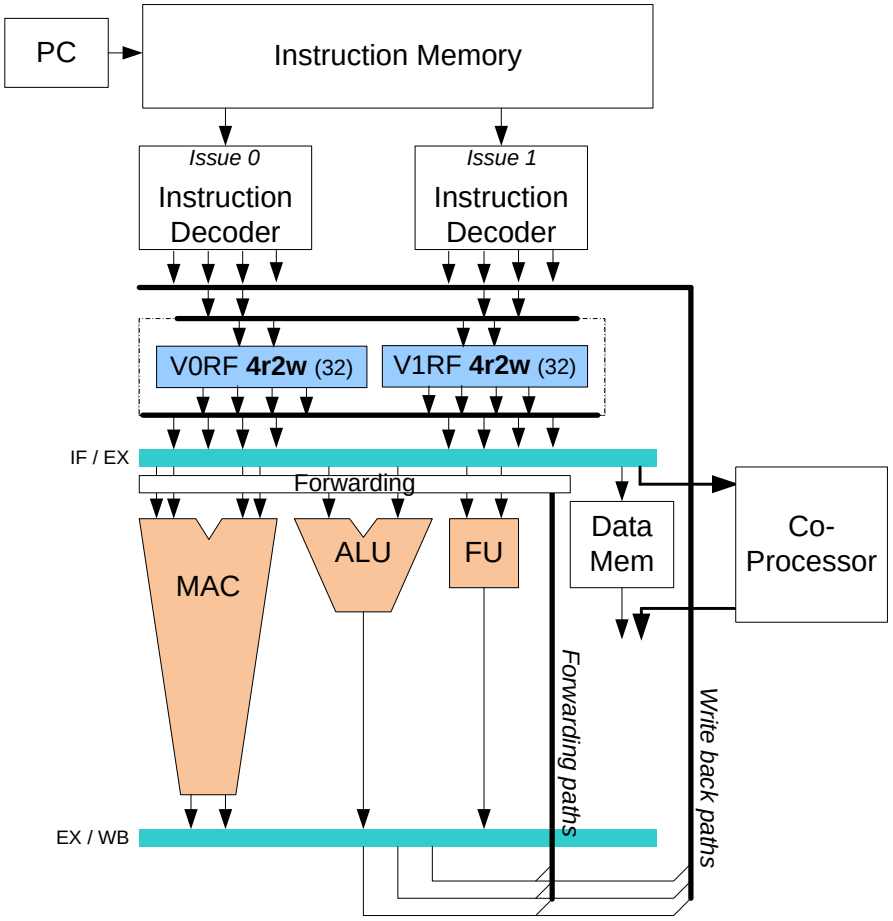
- Baseline **KAVUAKA** Architecture



[Hartig, Payá Vayá, et al. (2014) *"Customizing a VLIW-SIMD Application-Specific Instruction-Set Processor for Hearing Aid Devices"*, SiPS]

The KAVUAKA Hearing Aid Processor (II)

- Baseline **KAVUAKA** Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism



[Gerlach, Payá-Vayá, et al. (2017) *"Analyzing the Trade-Off between Power Consumption and Beamforming Algorithm Performance using a Hearing Aid ASIP"*, SAMOS]

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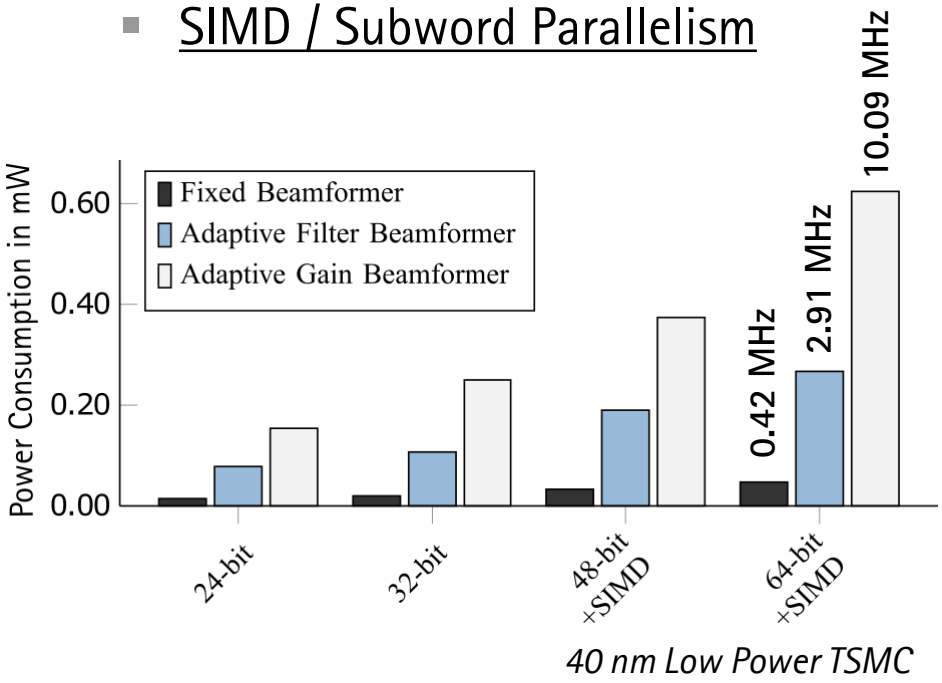
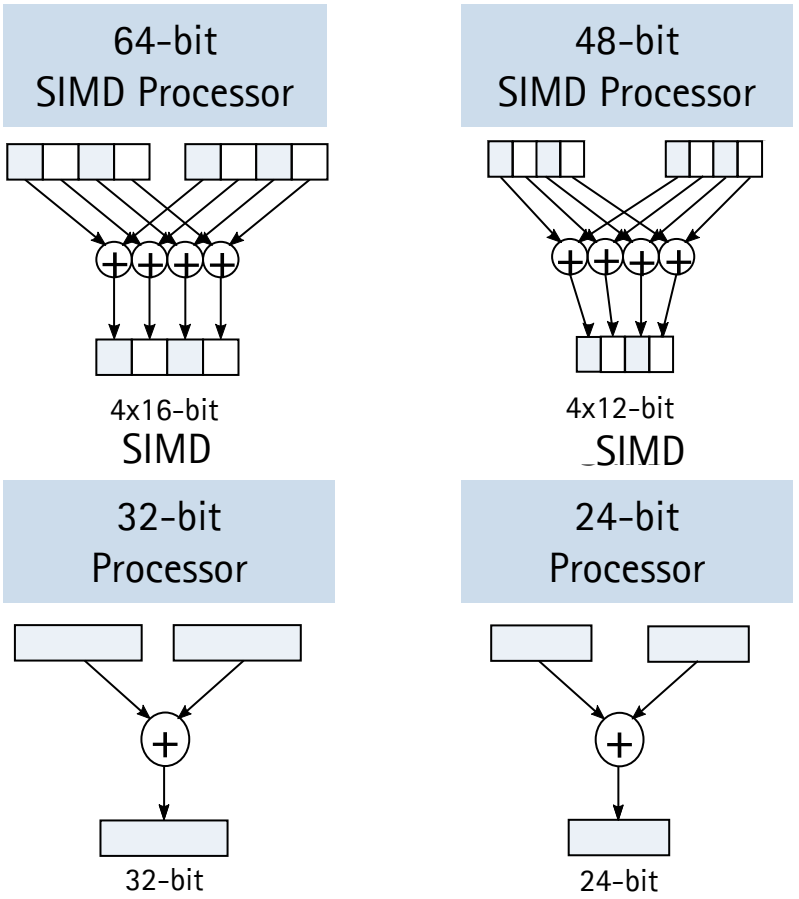
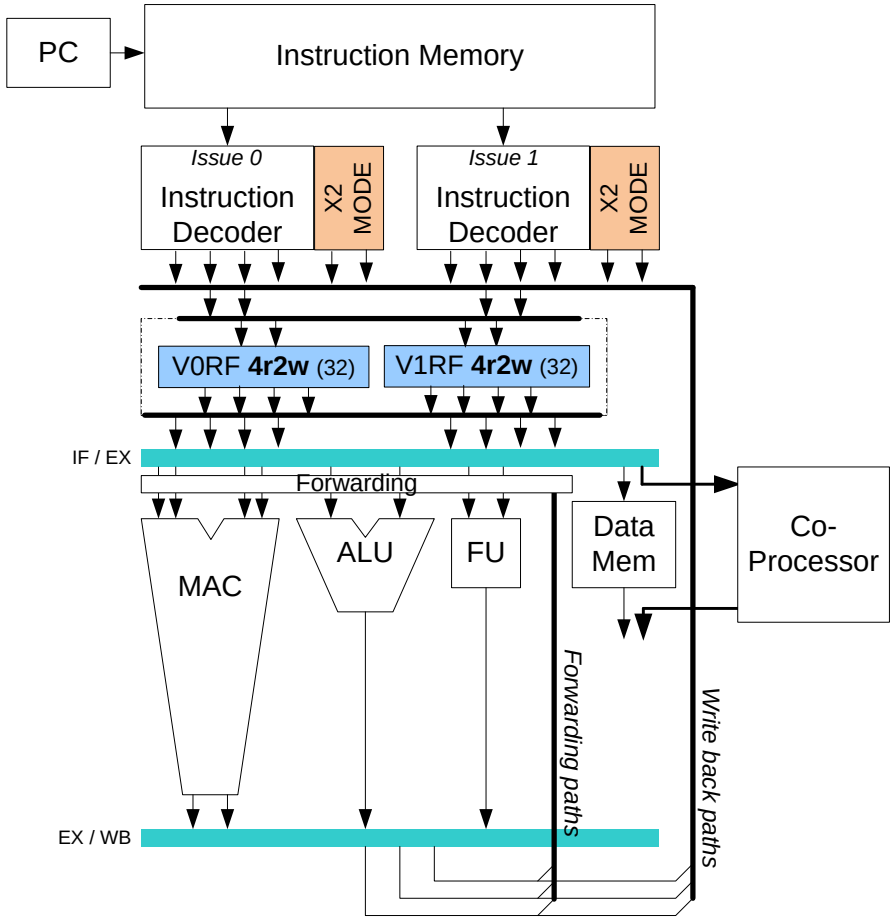




[Gerlach, Payá-Vayá, et al. (2017) *"Analyzing the Trade-Off between Power Consumption and Beamforming Algorithm Performance using a Hearing Aid ASIP"*, SAMOS]

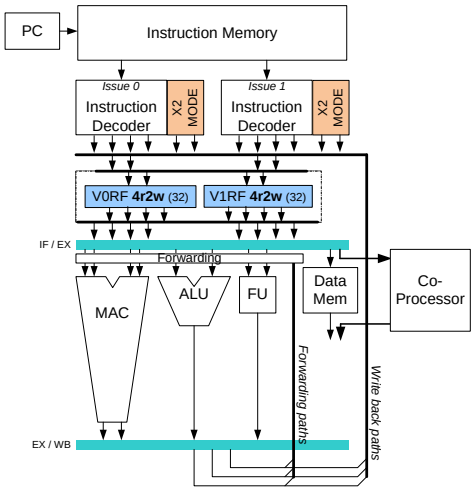
The KAVUAKA Hearing Aid Processor (III)

- Baseline **KAVUAKA** Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)



[Payá-Vayá, et. al. (2009) *"Instruction Merging to Increase Parallelism in VLIW Architectures"*, SoC]

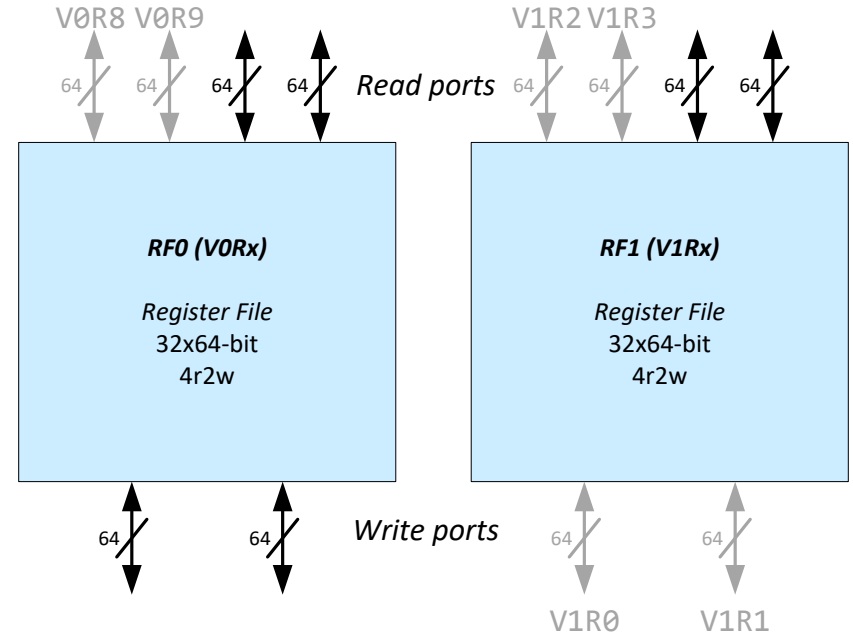
The KAVUAKA Hearing Aid Processor (III)




```
ADD V0R0, V0R2, V0R4
ADD V0R1, V0R3, V0R5
SR  V1R0, V0R8, V1R2
SR  V1R1, V0R9, V1R3
...
```

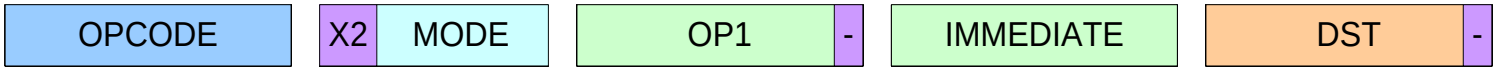
Assembler source code

Instruction scheduling




```
(0x00) ADD V0R0, V0R2, V0R4; ADD V0R1, V0R3, V0R5
(0x01) SR  V1R0, V0R8, V1R2; SR  V1R1, V0R9, V1R3
```

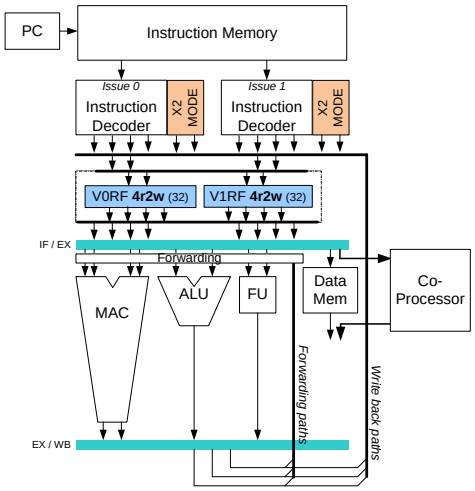
after scheduling



The KAVUAKA Hearing Aid Processor (III)

```
ADD_X2 V0R0+V0R1, V0R2+V0R3, V0R4+V0R5
SR_X2  V1R0+V1R1, V0R8+V0R9, V1R2+V1R3
...
```

Assembler source code



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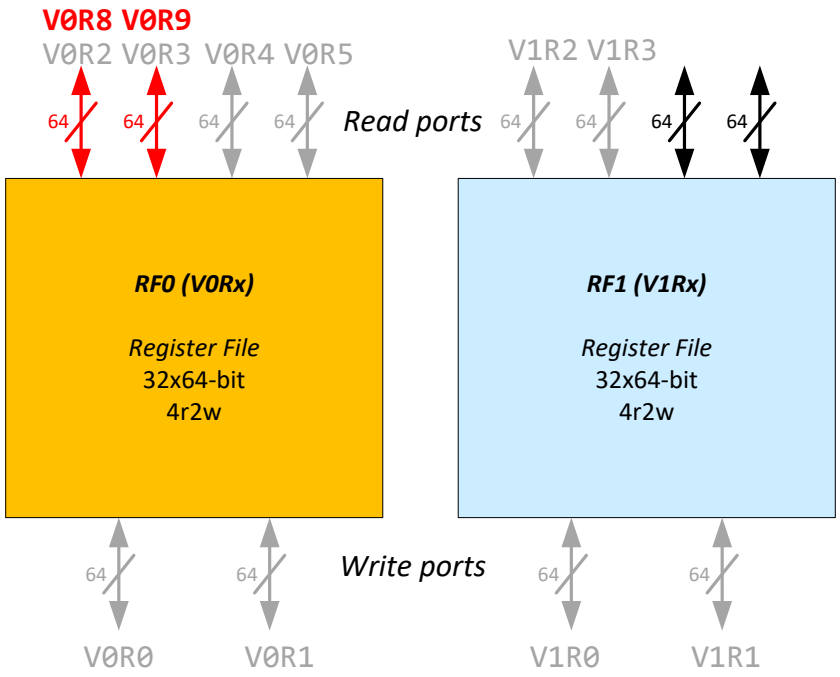
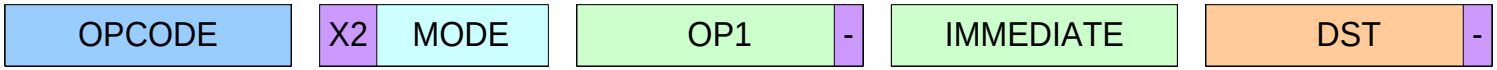



```
(0x00) ADD_X2 V0R0+V0R1, V0R2+V0R3, V0R4+V0R5; SR ..
(0x01) SR_X2  V1R0+V1R1, V0R8+V0R9, V1R2+V1R3; NOP
```

NOP

after scheduling



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ADD_X2 V0R0+V0R1, V0R2+V0R3, V0R4+V0R5
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```

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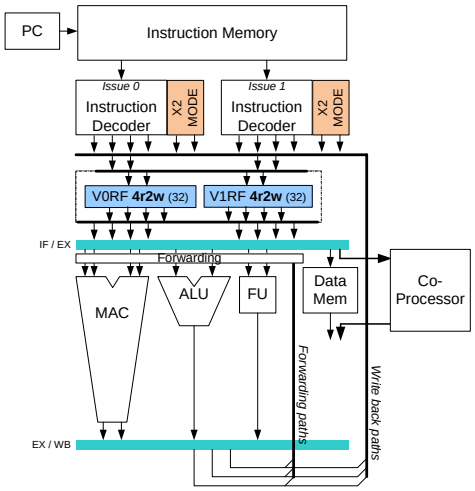

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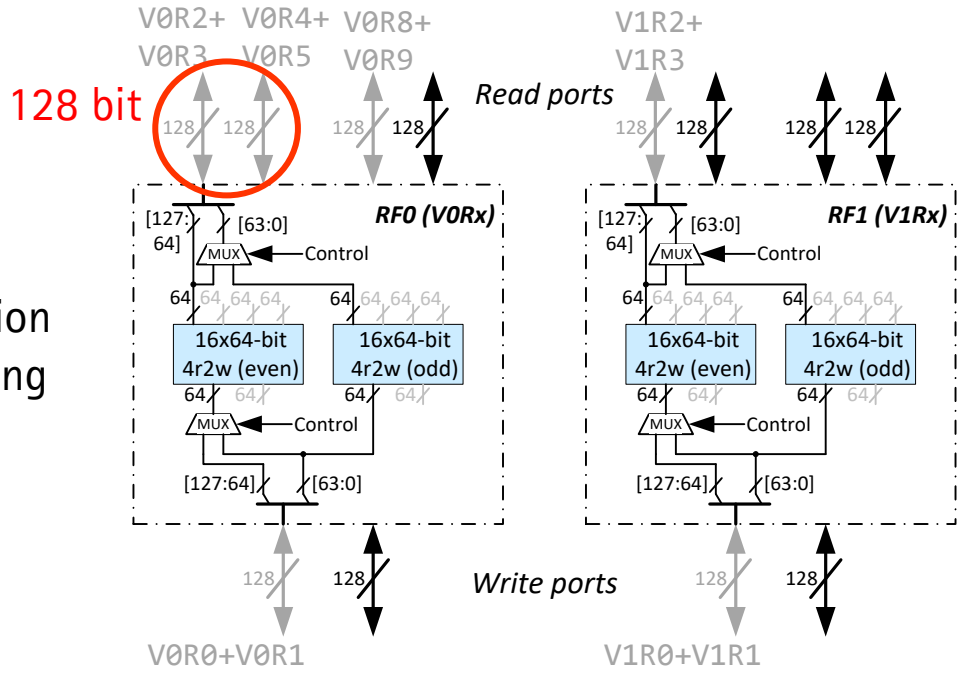
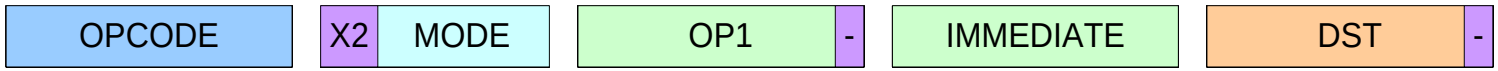
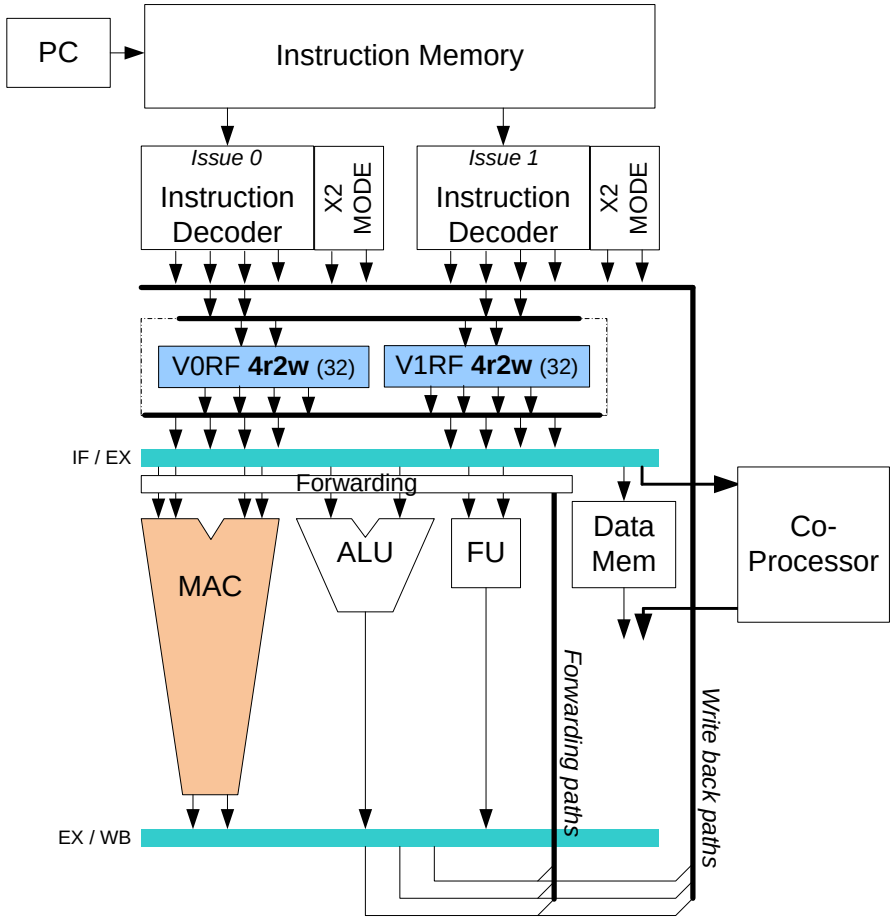



```
(0x00) ADD_X2 V0R0+V0R1, V0R2+V0R3, V0R4+V0R5; SR_X2  V1R0+V1R1, V0R8+V0R9, V1R2+V1R3
```



The KAVUAKA Hearing Aid Processor (V)

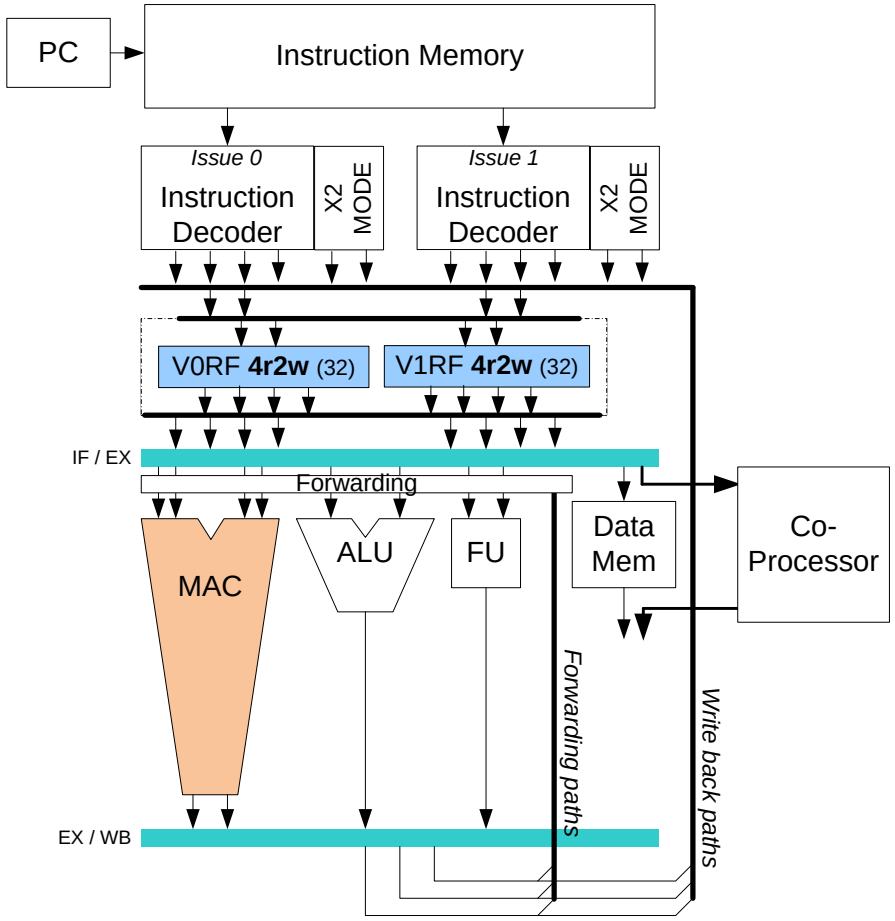
- Baseline **KAVUAKA** Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic using SIMD Mechanism



[Hartig, Payá-Vayá, et. al. (2014) *"Customizing a VLIW-SIMD Application-Specific Instruction-Set Processor for Hearing Aid Devices"* SiPS]
[Gerlach, Payá-Vayá, et al. (2016) *"Efficient Emulation of Floating-Point Arithmetic on Fixed-Point SIMD Processors"* SiPS]

The KAVUAKA Hearing Aid Processor (VI)

- Baseline **KAVUAKA** Architecture
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic
  - Complex-valued MAC



[Gerlach, Payá-Vayá, et al. (2015) *"An Area Efficient Real- and Complex-Valued Multiply-Accumulate SIMD Unit for DSPs"*, SiPS]

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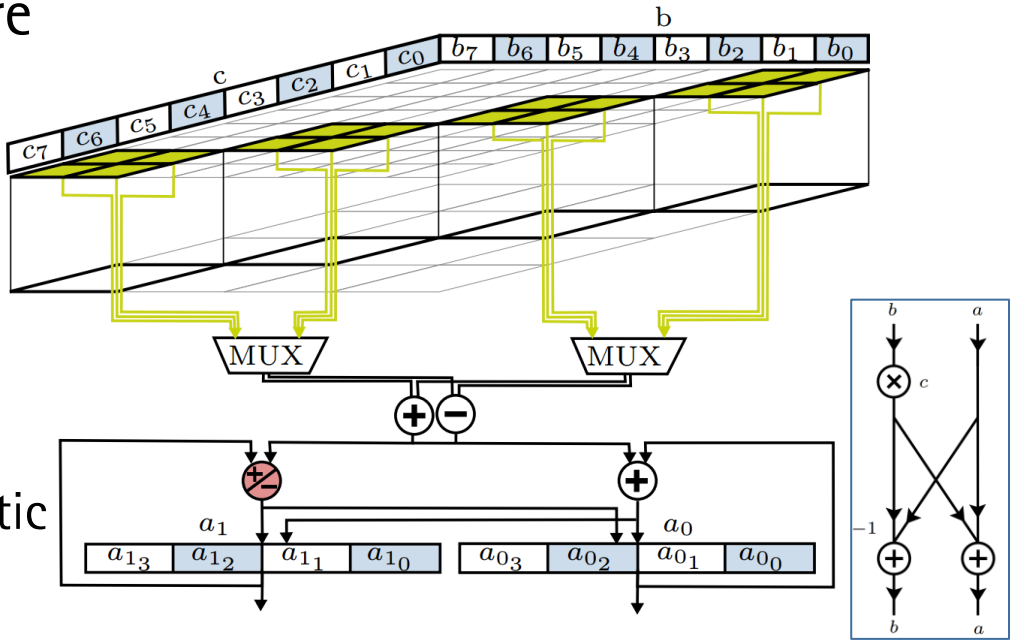

Processor: KAVUAKA	**32 Point FFT Cycles**	**Core Area** (*40 nm Low Power TSMC*)
Real-valued SIMD MAC	570	0.237 mm^2
Real- and Complex-valued SIMD MAC and Butterfly Operations	135 (Speedup: 4.22 x)	0.255 mm^2 (Overhead: 7%)

[Gerlach, Payá-Vayá, et al. (2015) *"An Area Efficient Real- and Complex-Valued Multiply-Accumulate SIMD Unit for DSPs"*, SiPS]

The KAVUAKA Hearing Aid Processor (VI)

MAC Arch.	Name	Clock frequency [MHz]	Number of MACs	Word/Subword [bit]	FFT Points 256 [cycles]
Single MAC	CFX [4]	300	2	24/24	8393 (438%)
	C55x [5]	200	2	16/16	4786 (250%)
	ADSP-21161N [6]	100	2	32fl	4316 (225%)
SIMD MAC	C674x [9]	456	2	32/32	2216 (116%)
	Nadehara [10]	200	1	64/16	4093 (214%)
	SC3850 [11]	1000	4	64/16	2587 (135%)
SIMD CMAC	**KAVUAKA**	**50**	**1**	**64/32**	**1915 (100%)**

[Gerlach, Payá-Vayá, et al. (2015) *"An Area Efficient Real- and Complex-Valued Multiply-Accumulate SIMD Unit for DSPs"*, SiPS]

The KAVUAKA Hearing Aid Processor (VII)

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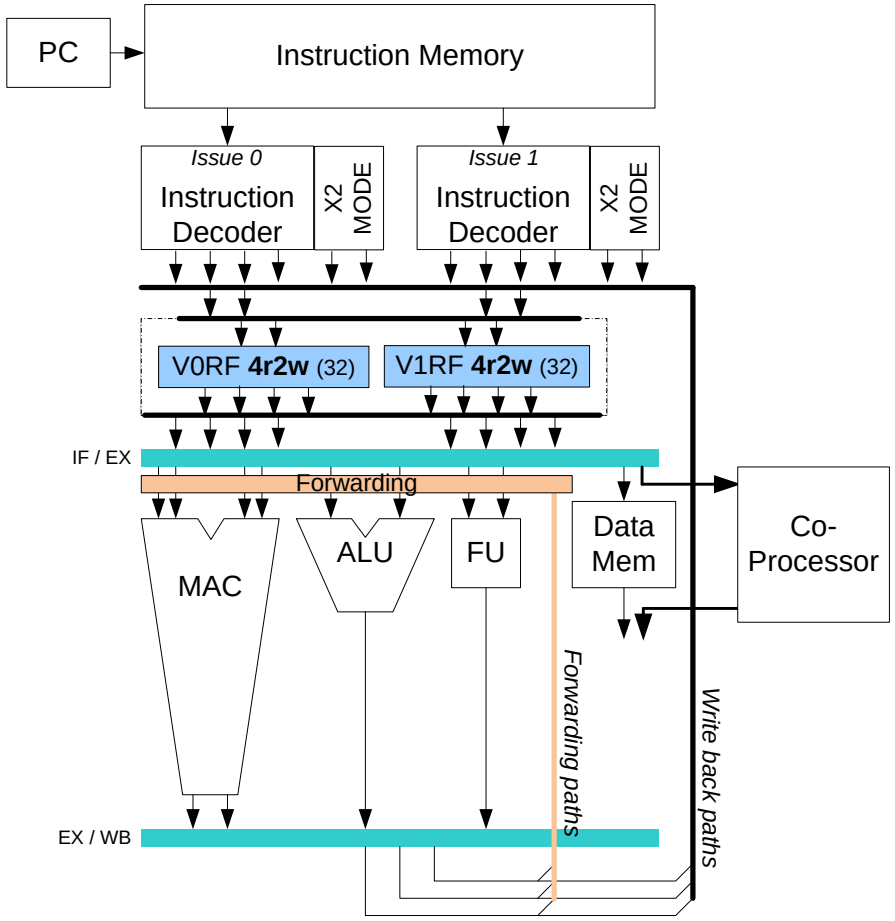
- Parallelization Techniques
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic
  - Complex-valued MAC
  - RF Isolation and Forwarding



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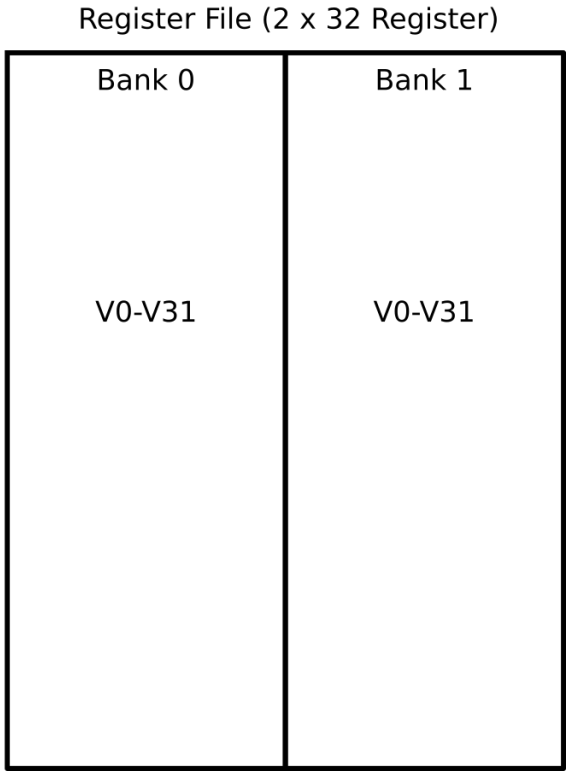
The KAVUAKA Hearing Aid Processor (VII)



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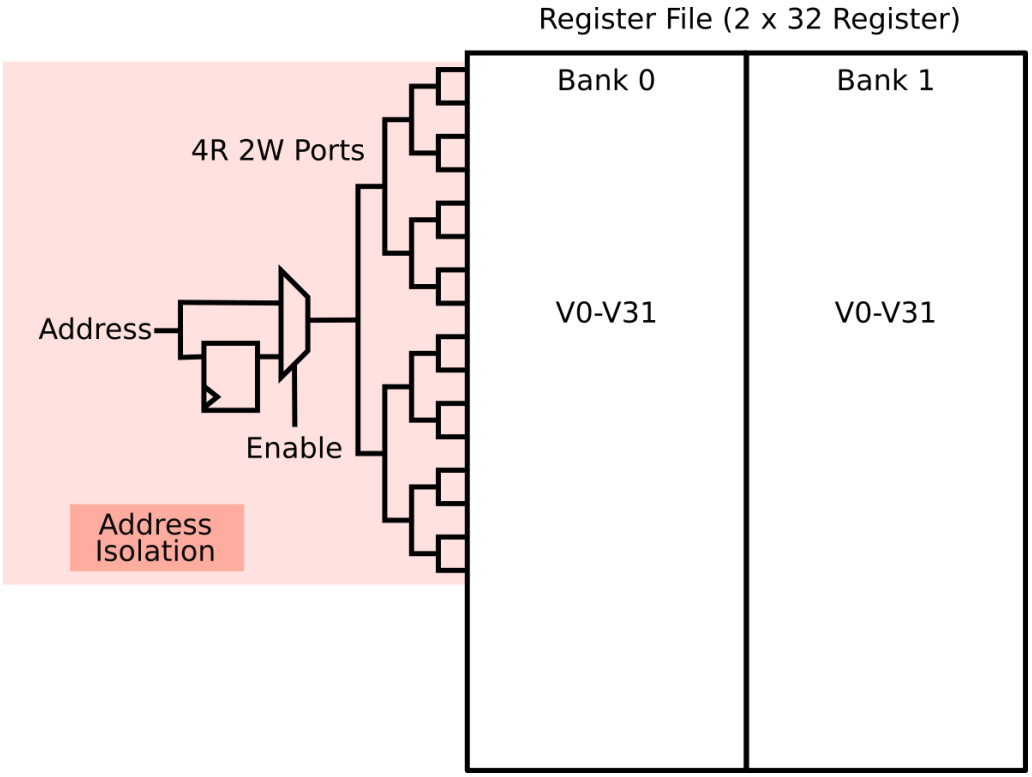
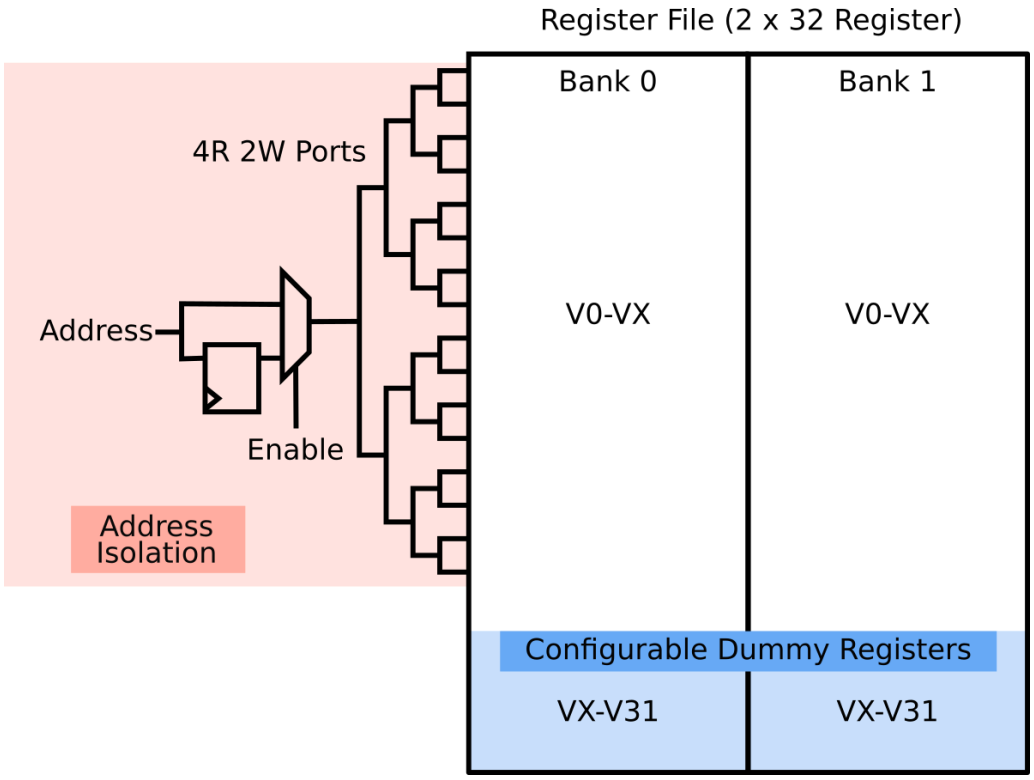
The KAVUAKA Hearing Aid Processor (VII)



The KAVUAKA Hearing Aid Processor (VII)



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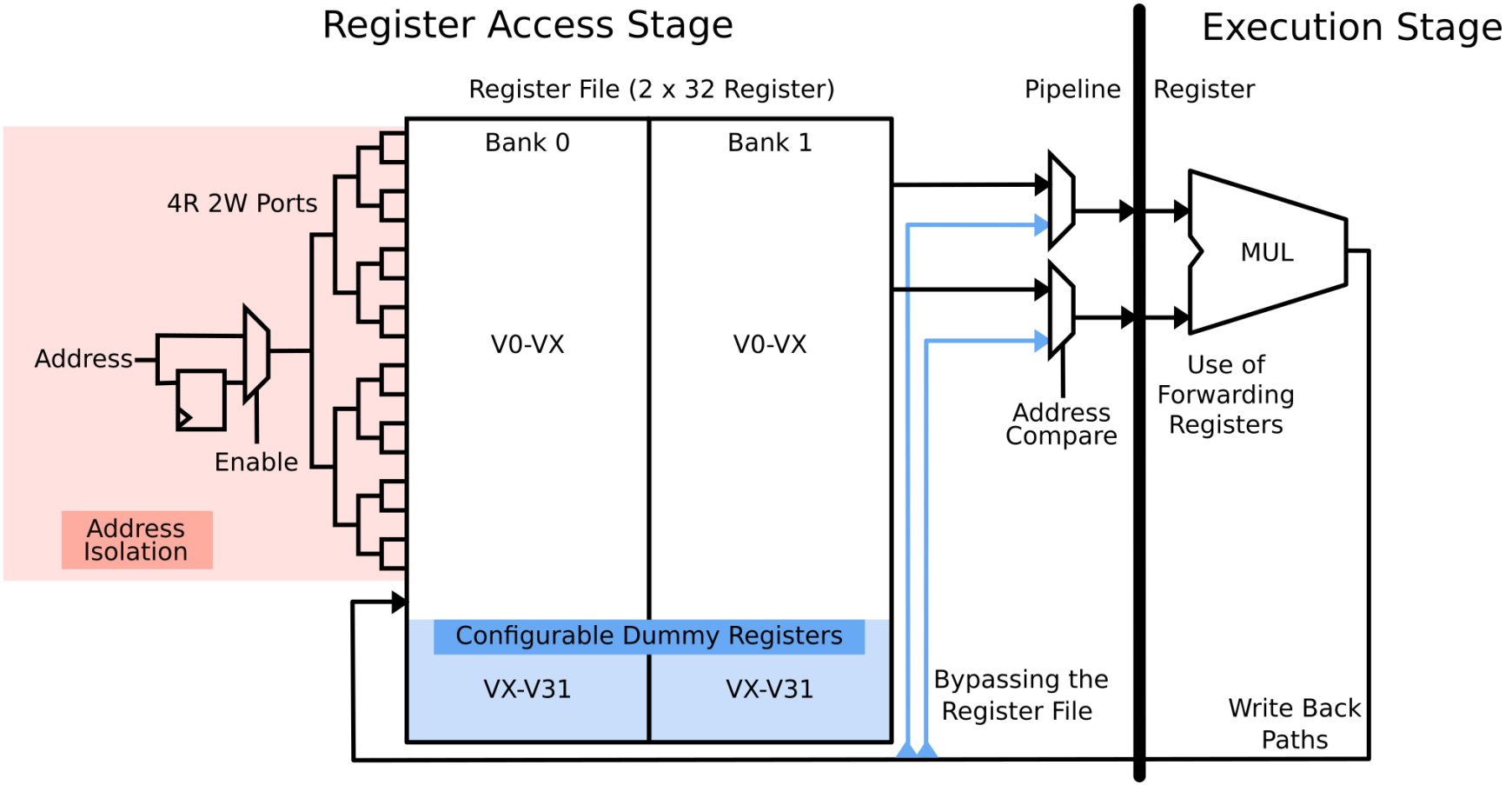
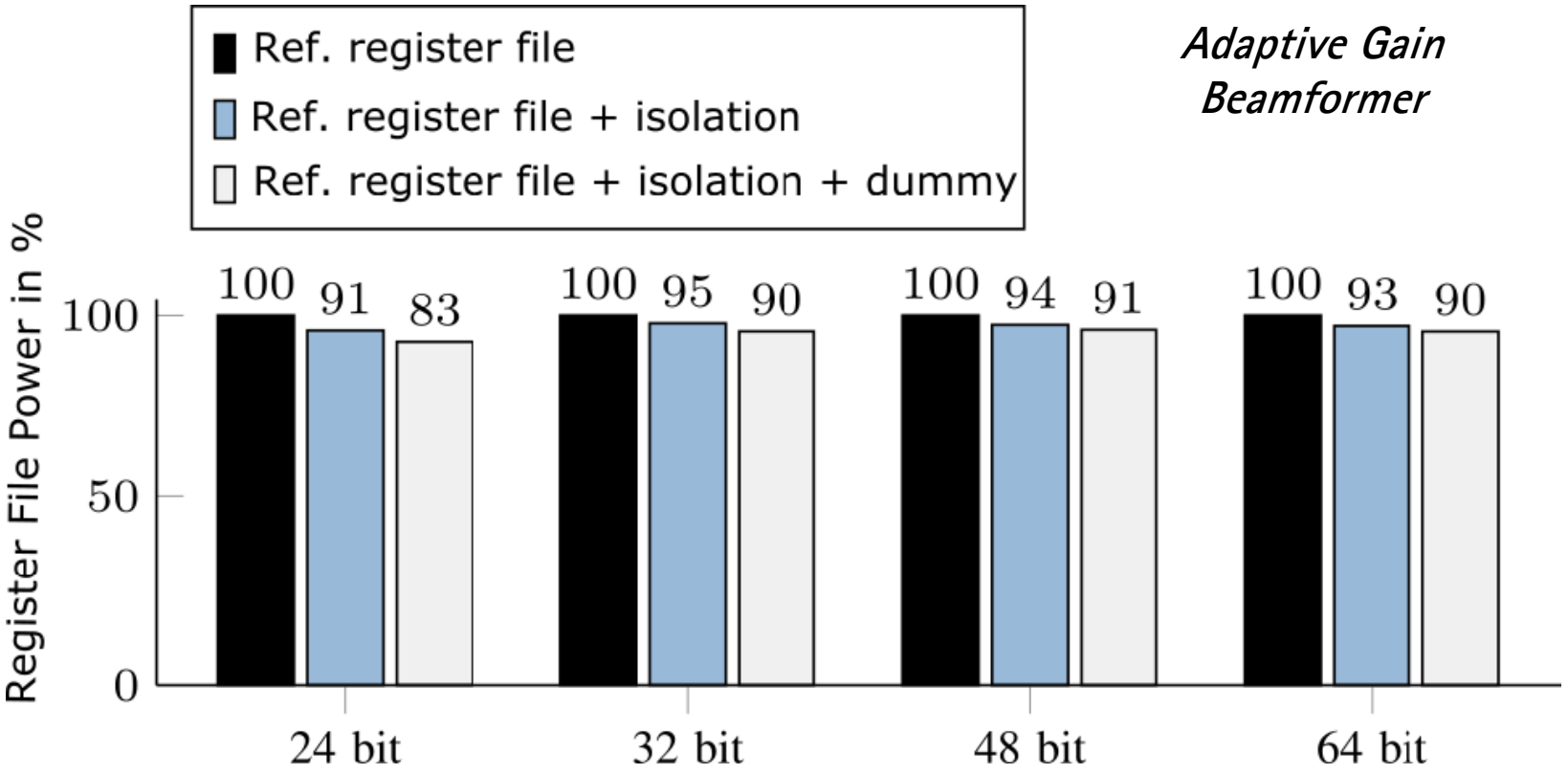


The KAVUAKA Hearing Aid Processor (VII)



Adaptive Gain Beamformer

40 nm Low Power TSMC

The KAVUAKA Hearing Aid Processor (VIII)

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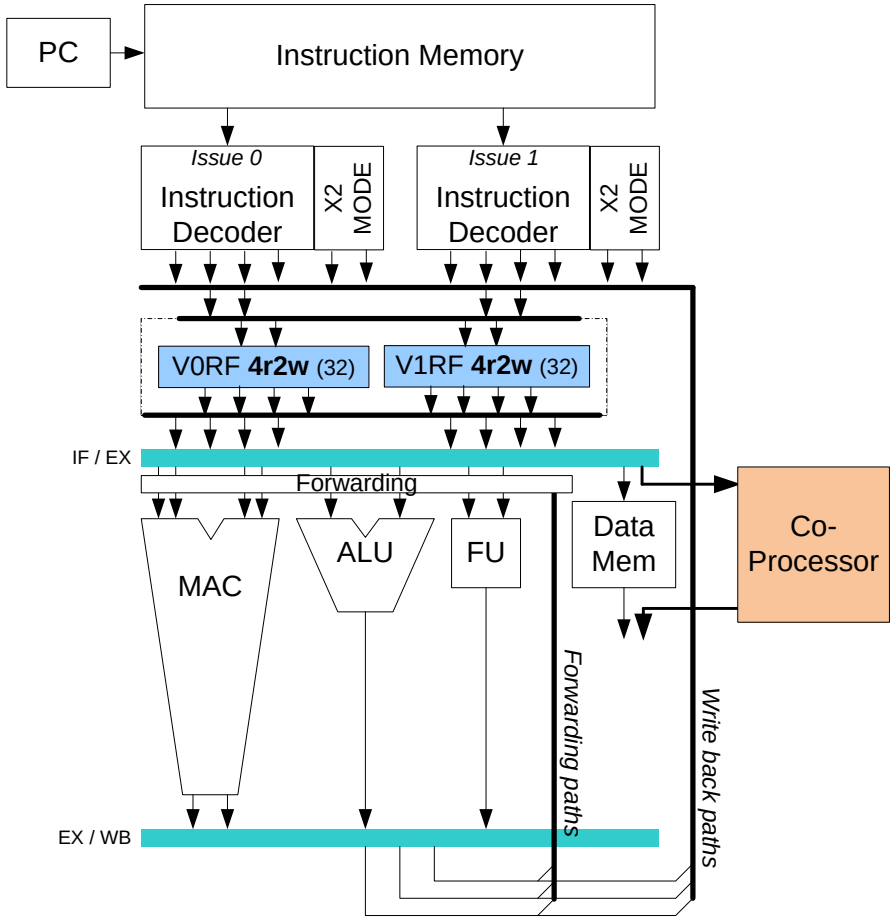
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic
  - Complex-valued MAC
  - RF Isolation and Forwarding
  - Co-processors



Gerlach, Payá-Vayá, et al. (2016) *"A Highly Optimized Arithmetic Software Library and Hardware Co-processor IP for Fixed-Point VLIW-SIMD Processor Architectures"*, Technology Transfer in Computing Systems (TETRACOM Technology Transfer Project)

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- Baseline **KAVUAKA** Architecture
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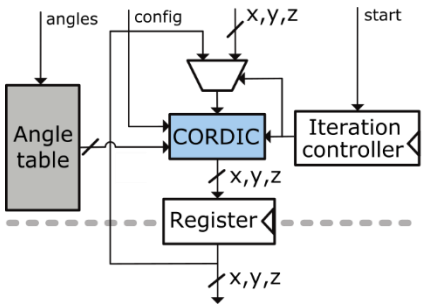
- Specialization Techniques
  - Complex Addressing Mode

HW



SW

```
MVI_32  VxR70, #1
ANDCS_32 VxR70, VxR70, SHIFT_CNT
SMVI CONDSEL, #0b0010  // COND_Z
MIXL_32 VxR54, VxR53, VxR53
MIXR_32 VxR70, VxR53, VxR53
MVCR_32 VxR54, VxR70
SMVI VxR98, REG_Z_OUT, #0
CONDSEL, #0b0011  // COND_N
SUBICS_32
// Kernel equations
// x = x - sigma * 2^(-iteration) * y
// y = y + sigma * 2^(-iteration) * x
```

Fast computations of non-linear functions

Hyperbolic and trigonometric operations		Sine	Cosine	Exponential	Natural logarithm	Square root
Cycles	KAVUAKA+CORDIC (HW)	71	71	76	56	59
	KAVUAKA (SW)	621	621	668	664	649
	TI TMS320C6478	1259	1523	1529	1134	341

Gerlach, Payá-Vayá, et al. (2016) *"A Highly Optimized Arithmetic Software Library and Hardware Co-processor IP for Fixed-Point VLIW-SIMD Processor Architectures"*, Technology Transfer in Computing Systems (TETRACOM Technology Transfer Project)

The KAVUAKA Hearing Aid Processor (IX)

- Baseline **KAVUAKA** Architecture
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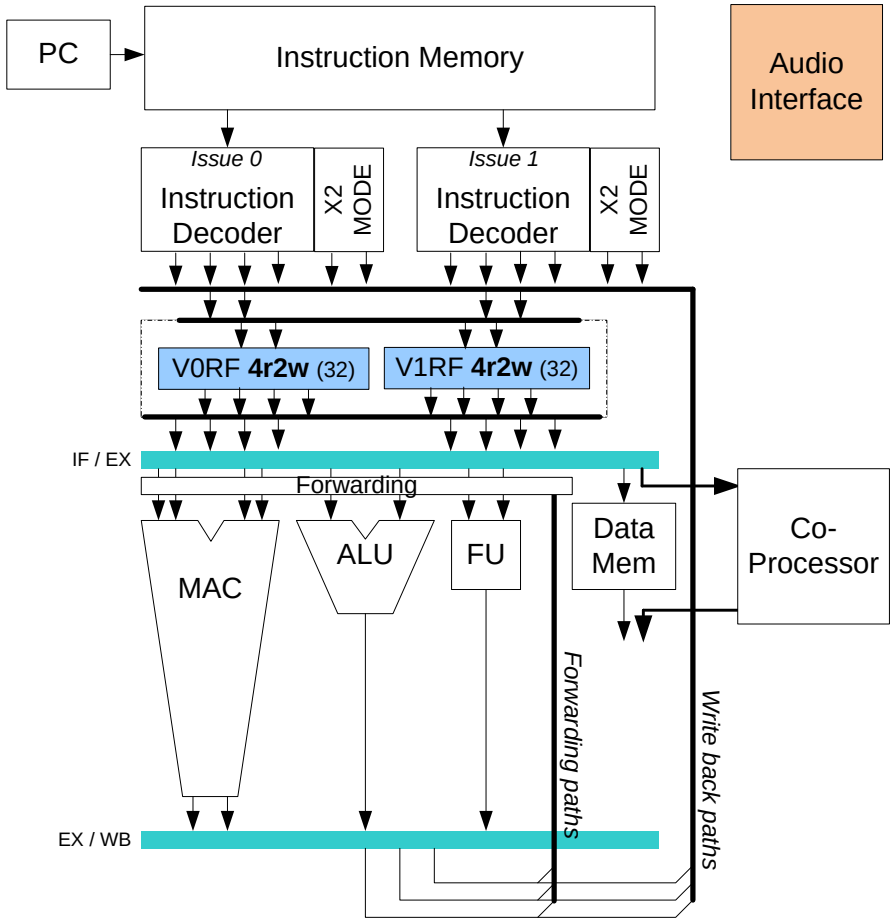
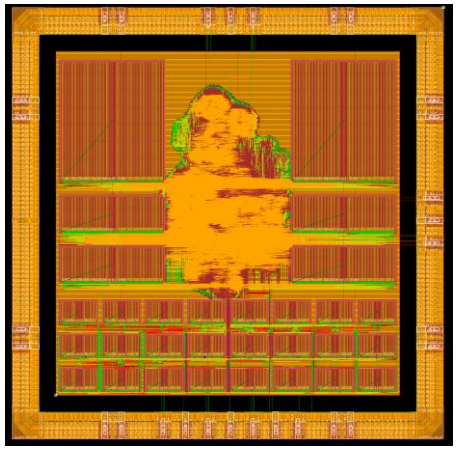
  - SIMD / Subword Parallelism
  - Instruction Merging (X2-MODE)
- Specialization Techniques
  - Complex Addressing Mode
  - Emulated Floating-Point Arithmetic using SIMD Mechanism
  - Complex-valued MAC
  - RF Isolation and Forwarding
  - Co-processors
  - Low latency audio interface



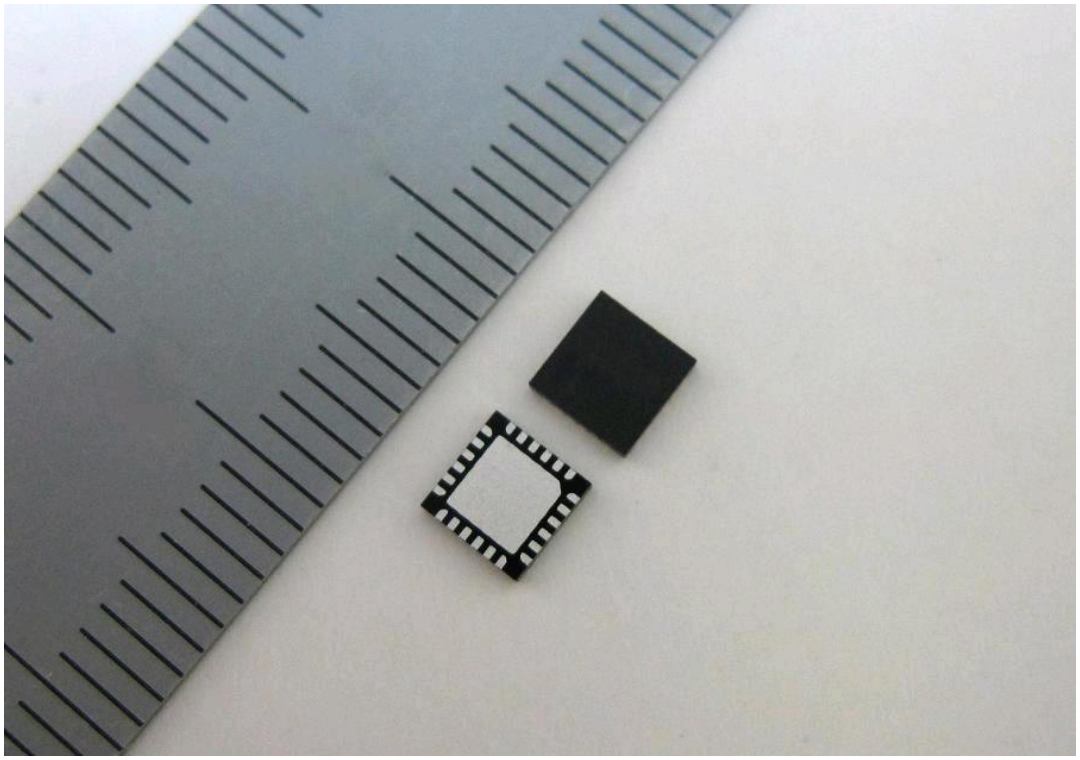
Gerlach, Payá-Vayá, et al. (2016) *"A Low Latency Multichannel Audio Interface for Low Power SIMD Digital Signal Processors"*, ICT.OPEN

The KAVUAKA Hearing Aid Processor (X)
A Digital Hearing Aid Application-Specific Processor



- **KAVUAKA Processor (Big Configuration)**
  - VLIW: 2-issue-slots (+ 2 instruction merging)
  - SIMD: 64-bit or 2x32-bit or 4x16-bit or 8x8-bit
  - Max. Frequency: 75 MHz
  - TSMC 40 nm Low Power Technology
  - Estimated Silicon Area : **0.922 mm²** **< 1 mm²**
  - Estimated Power Consumption: **0.635 mW** **< 1 mW**
- **Test Chip**
  - Available Silicon Area : **3.9 mm²**
  - 2 Cluster each with 2 KAVUAKA and 10 Co-Processors

The KAVUAKA SoC



- The manufacturing is scheduled within the next possible tape-out run, which is expected to take place 06/03/2018 and manufactured on 05/04/2018.

Thank you for the attention!