Enabling Connected Intelligence

22FDX for Cost-Effective Low Energy Designs

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GLOBALFOUNDRIES®

Realizing Cost-Effective Low Energy Designs

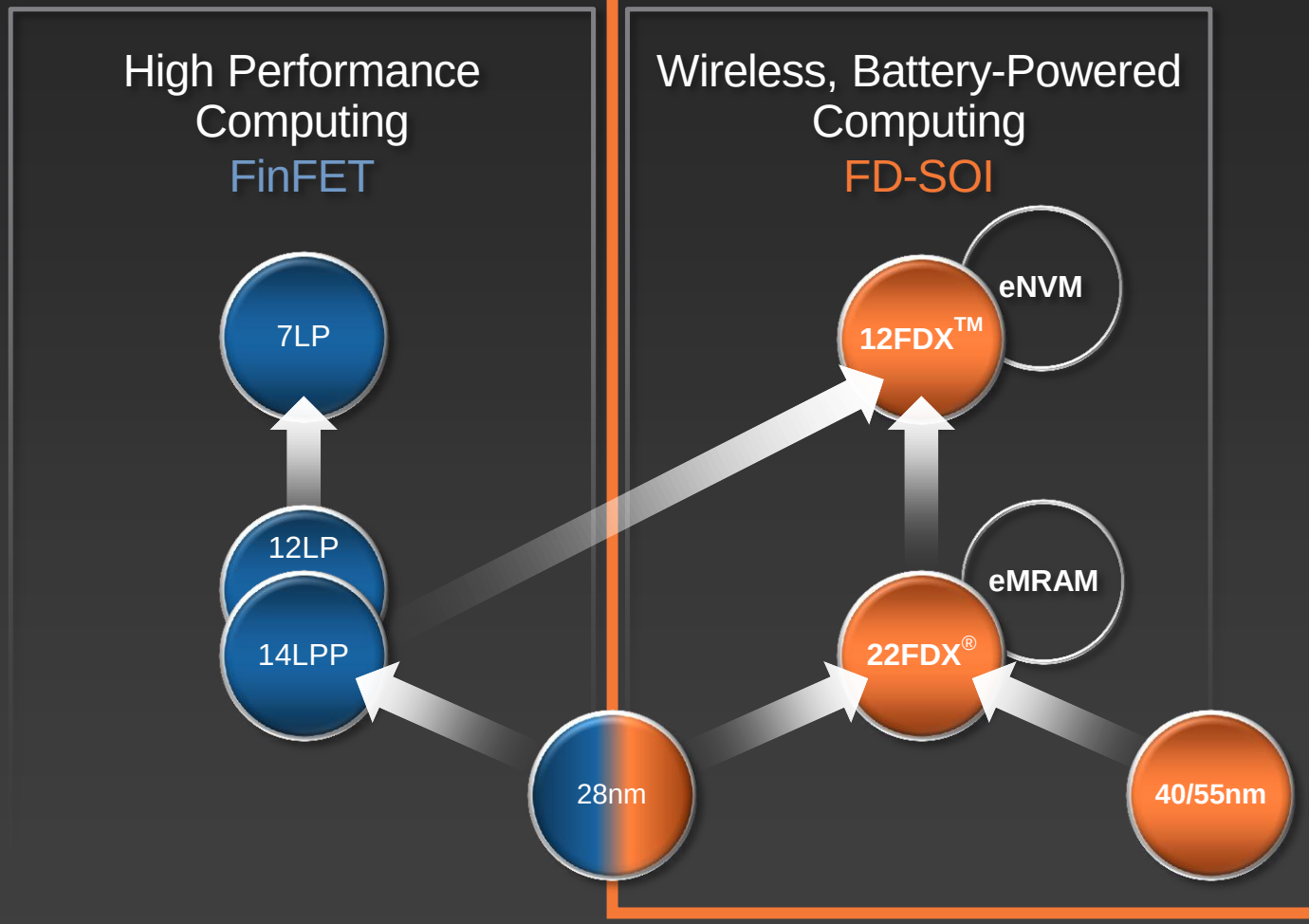
1. 22FDX® Technology & Enablement
2. 22FDX® with Back Gate Bias
3. 22FDX® Technology Benefits
4. 22FDX® Ecosystem Expansion

GF CMOS Roadmap Redefines Mainstream

Applications:
- Servers
- HPC
- Graphics
- High-end AP
- Core networking
- Auto high-end ADAS

Premium Tier

Features:
- High-performance
- Balanced-cost



Applications:
- Low & mid AP
- IoT
- Autonomous vehicles
- Mobile camera

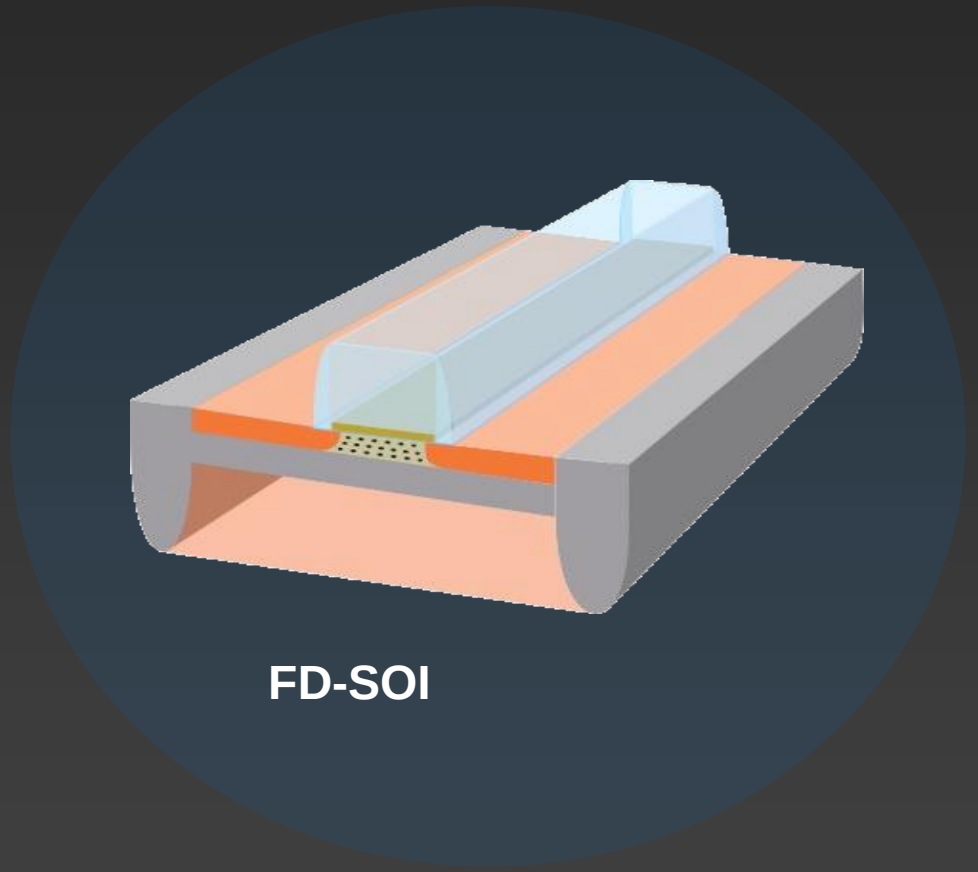
Volume Tier

Features:
- Low-power
- Cost-effective performance
- High Performance RF and mmWave
- Embedded memory

22FDX® Platform from GLOBALFOUNDRIES

- Architected for:
  - FinFET performance at 28nm die cost
  - Emerging products in IoT, Mobile, and RF

- Enables differentiated customer solutions
  - Software-controlled body-bias
  - Energy efficiency
    - Ultra-low voltage (0.4V)
    - Ultra-low leakage (1pA/µm)
  - RF integration with high f_T/f_{MAX}
  - Integrated power management



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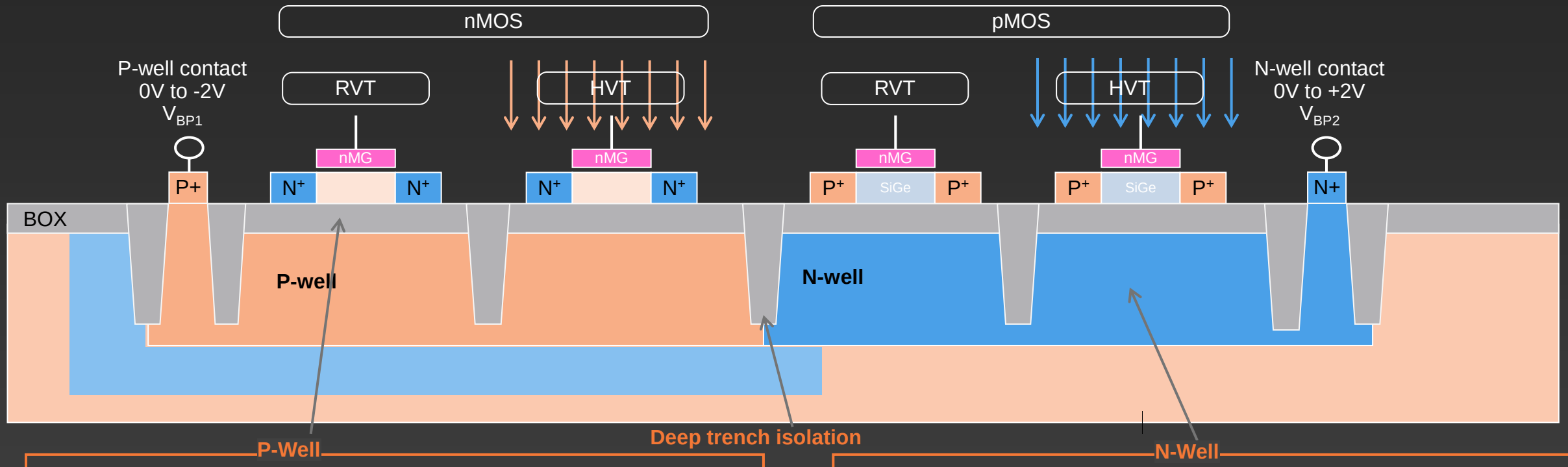
Reverse Back Bias Blocks

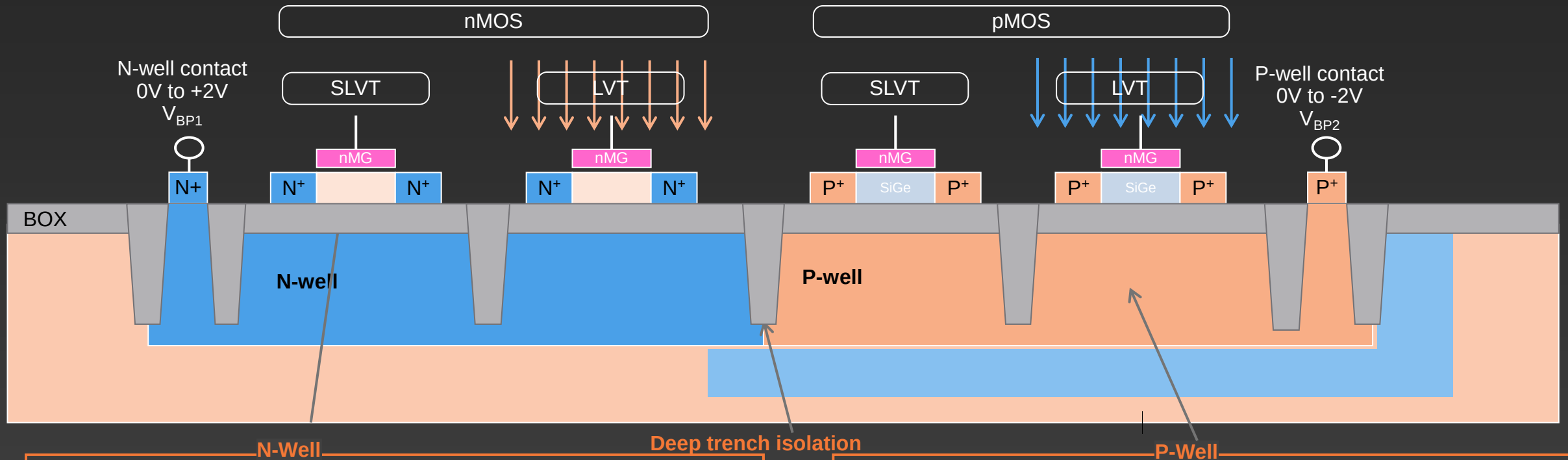


Within a P-well, the flavor of the transistors can be changed by using a lightly p-doped channel implant

Within a N-well, the flavor of the transistors can be changed by using a lightly n-doped channel implant

- RVT/HVT are **swappable post PnR** without area scaling impact
- **Full RBB capability** is possible with standard well scheme
- Gate length sizing for **additional Vt/Ioff control**

Forward Body Bias Blocks



Within a N-well, the flavor of the transistors can be changed by using a lightly p-doped channel implant

Within a P-well, the flavor of the transistors can be changed by using a lightly n-doped channel implant

- SLVT/LVT are **swappable post PnR** without area scaling impact
- **Full FBB capability** is possible with flip-well scheme
- Gate length sizing for **additional Vt/Ioff control**

Body Bias Value Proposition – ‘Trim’ & ‘Boost’

- Compensate for process, temperature, and aging variations

  Benefits:

  - Reduce Area
  - Reduce Power
  - Enables Ultra Low Voltage Operation

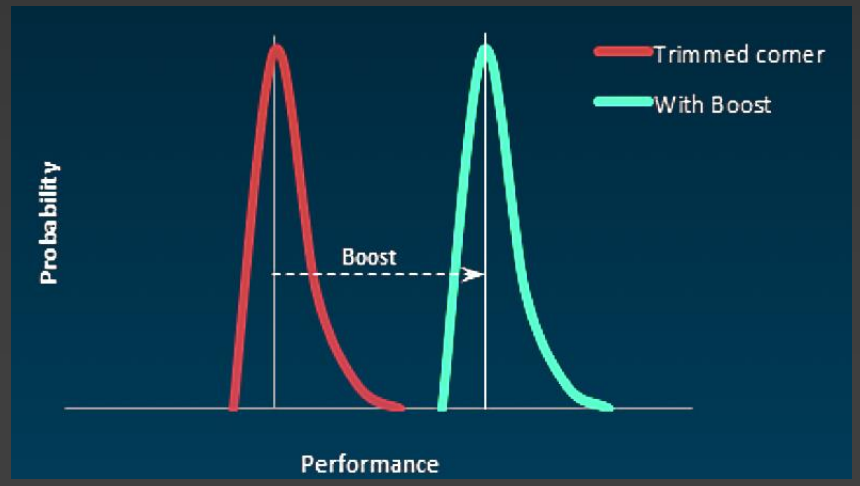
- Boost Performance to FinFET Speeds

  Benefits:

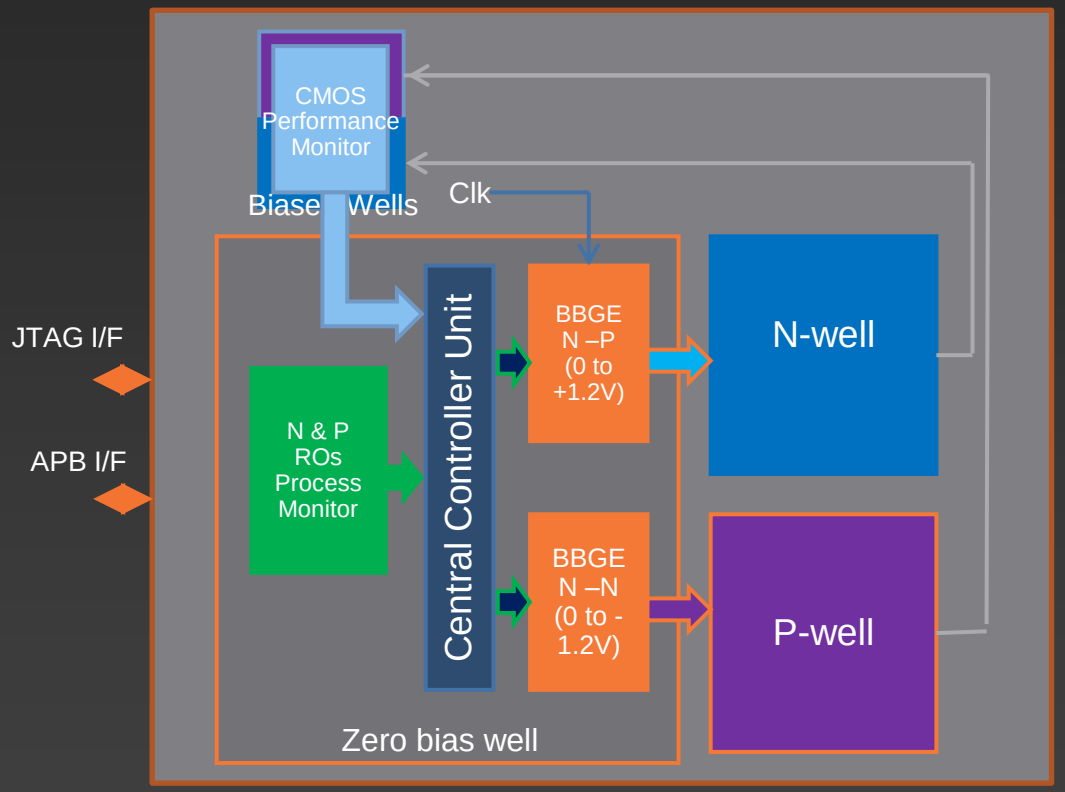
  - Increase Performance
  - Less Dynamic Power than Voltage Scaling

Global Corner Trimming

Performance Boost



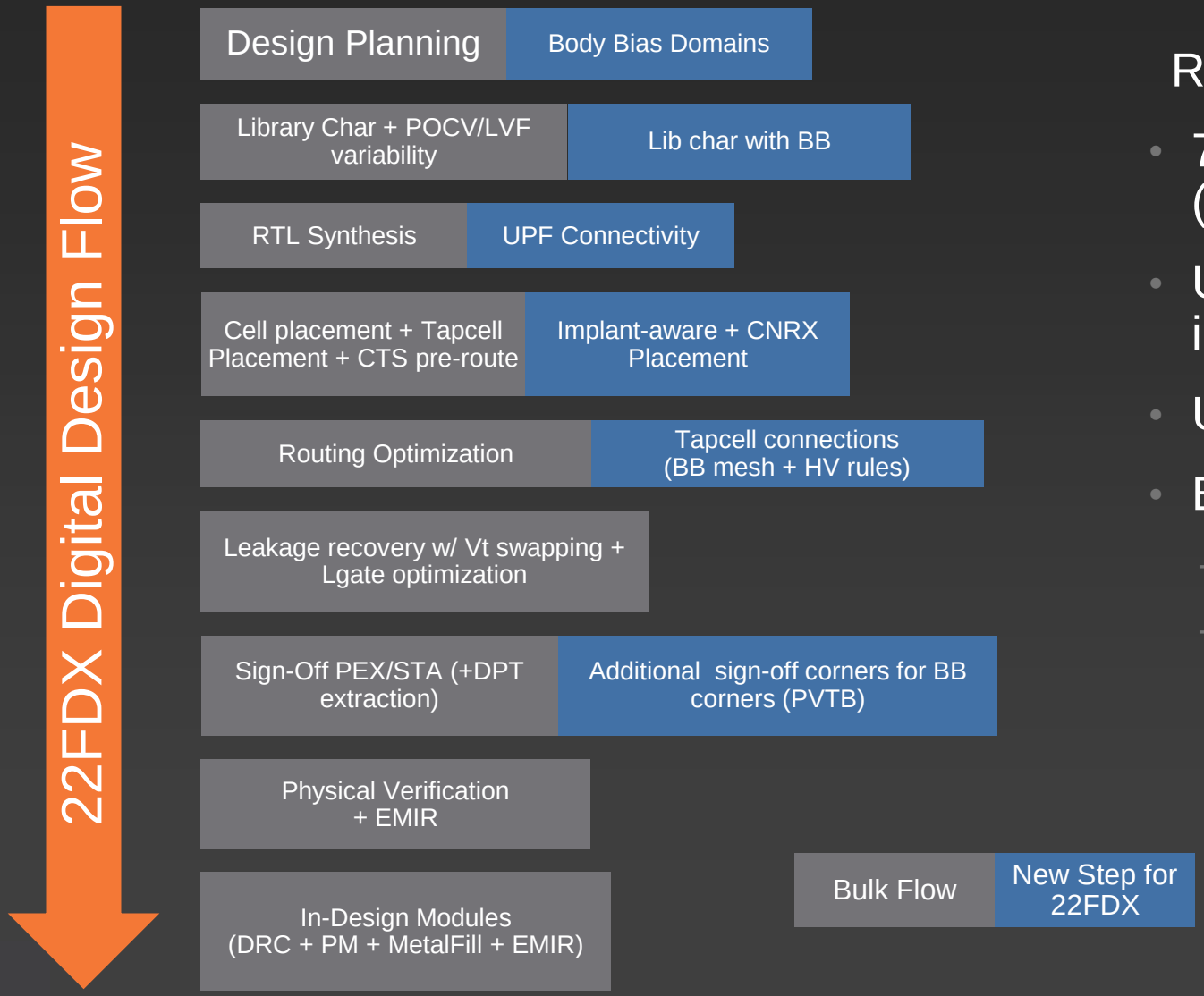
Dynamic Global Corner Trimming Solution for IoT



- **BBGEN IP**
  - Supports 1mm^2 to 5mm^2 well area
  - Input Clock: 25MHz to 100MHz
  - Supply: 0.65Vnom - 0.8Vnom
- **Process and Performance Monitors**
  - P-fet and N-fet RO's for initial bring-up and dynamic tuning
  - CMOS Performance Monitor for dynamic tuning based on process and temperature
- **APB interface** for user control of Bias Generator
- **JTAG interface** for observability and controllability during Testing
- **Ultra low voltage standard cell library**
- **Ultra low voltage memories**

22FDX® Ultra Low Power Reference Flow

Cadence and Synopsys Certified



Reference flow adapted to ULP library

- 7.5T, 116CPP physical design setup (units, track plan, PG mesh)
- ULP corner & margin setup for implementation and sign-off
- UPF set up
- Body bias physical design elements
  - Tap cell placement
  - BB net routing

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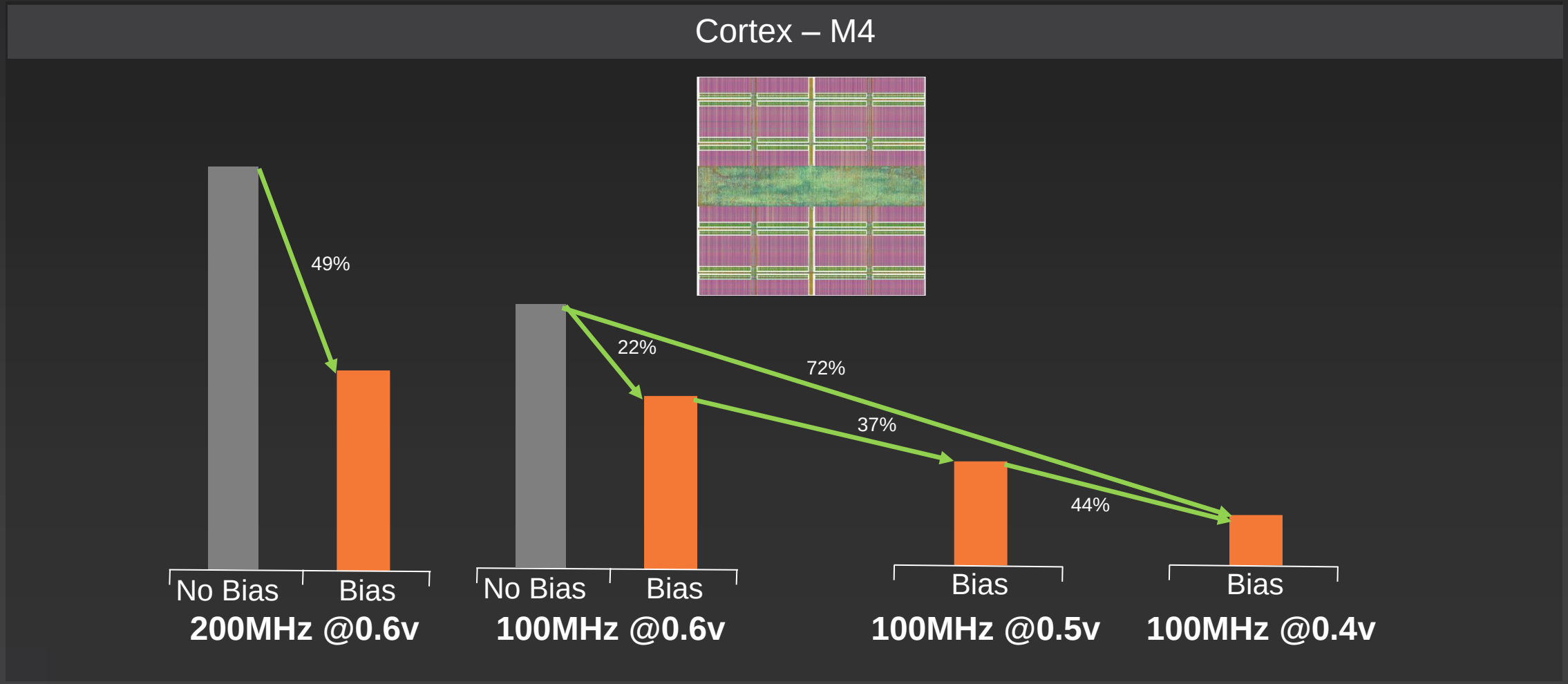
Arm® Cortex®-M4 – Back Gate Bias Benefit

72% Power Advantage achieved with Low Voltage and Bias Trimming



Bias-Trimming: Mixed Vt achieved > 300MHz at 0.4V, and a Customer Application is achieving > 500MHz at 0.4V.

22FDX - Demonstrator Description

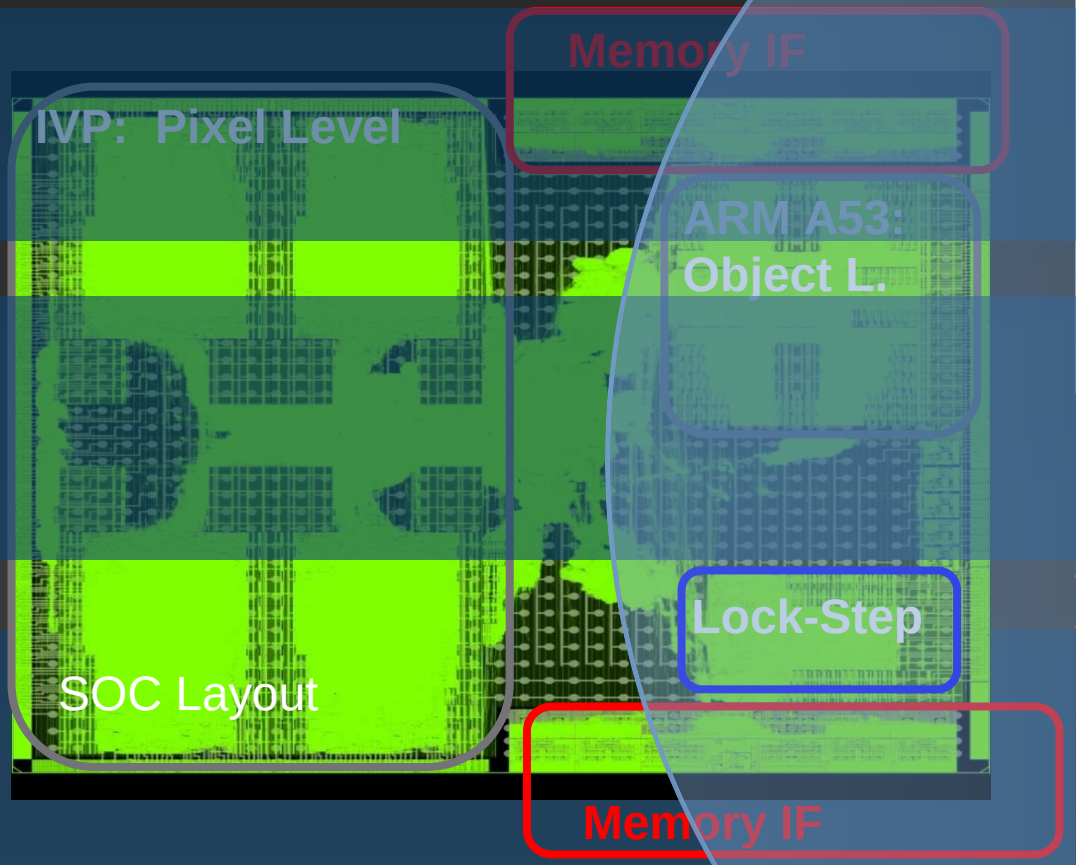
ADAS Demonstrator for image recognition / classification, image warping and Real-Time Processing

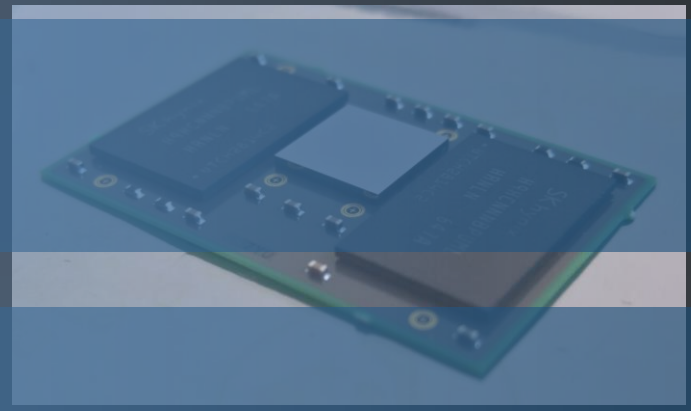
Collaboration Partners:

DREAMCHIP, CADENCE, INVECAS, GF, Arm, ArterisIP

Targeted Use-Cases:

- In-vehicel Image Processing
- Image recognition
- ADAS Development Platform
- Industrial Automation





System-Module (Chip + LPDDR4)

360° Surround View Demo Setup
Demo-Car with 4 cameras

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FDX™ Ecosystem

- Global Program FDXcelerator™
- Special Programs : Germany, Europe

IP, EDA, Design Services, ASICs, Reference Platforms, Packaging and Test Solutions

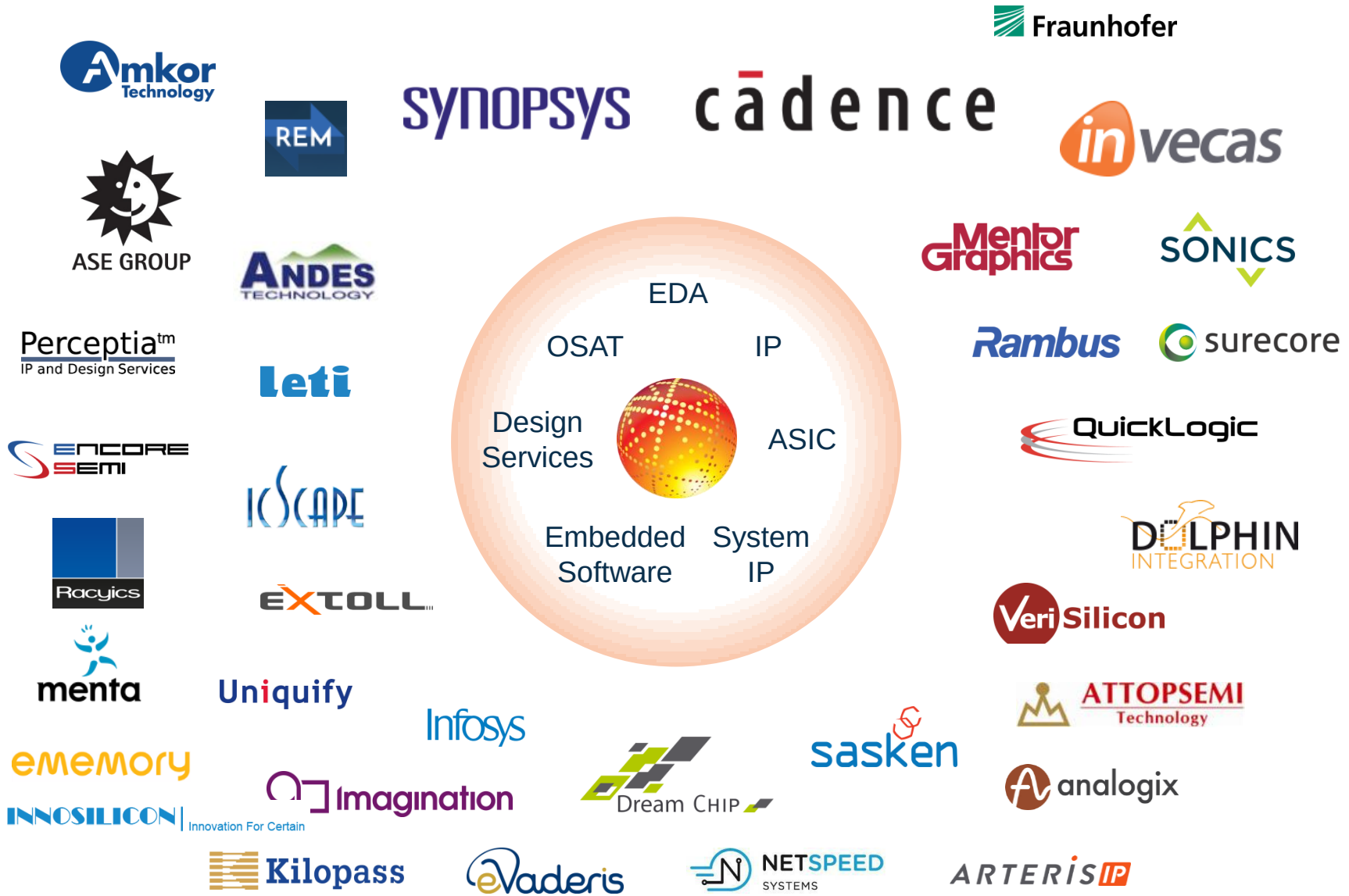
Design & Development	Manufacturing
Customers and FDX™ Ecosystem	*GLOBALFOUNDRIES*

FDXcelerator™ Ecosystem Partnering for Growth

Reduce time to market and facilitate FDX™ SoC product design

- Easy access to plug and play solutions
- Minimizes customer development costs
- Lowers barriers of migration

~ 40



Building Global Scale for FDX™

Govt, GF, Partners & Customers invest to expand FD-SOI ecosystem

- Commitment to regional growth
  - IP Development
  - Design Services
  - Fabless Companies
  - Training & Curriculum

Local Customer Benefits

- Local manufacturing
- Accelerate SoC TTM
  - Local capability & support
- Growth of engineering talent
- Expand Local semiconductor Innovation and expertise with strong government support

Dresden, Germany

45nm – 22nm

Dresden, Germany Fab 1

- Expanding 22FDX® FD-SOI capacity by 40% by 2020
- Developing derivatives (RF, Auto, eMRAM)

Chengdu, China

180nm – 12nm

Chengdu, China Fab 11

- New 300mm fab
- 180nm/130nm production starting 2H18
- FDX in 2H19

GLOBALFOUNDRIES and Academic Collaboration

Value creation through collaborative University programs

- Access to circuit design
- Access to global shuttles
- Customer and business opportunity focus
- Strong drive for innovation

Summary

- 22FDX® Platform is fully enabled with a Comprehensive IP Portfolio
- Back Gate Bias Trimming Solutions Methology available for benchmark Performance/Watt and Ultra-Low Power
- 22FDX: Proven SOC capability with ADAS Demonstrator
- 22FDX Ecosystem is thriving
  - Partners are delivering broad and unique solutions for 22FDX
  - Providing wide development / solution footprint

Thank you