



Martin Zeller (DCT)

# **SDIP ASIC Update Tensilica Day Hannover 2018**

## *DCT Company Profile*

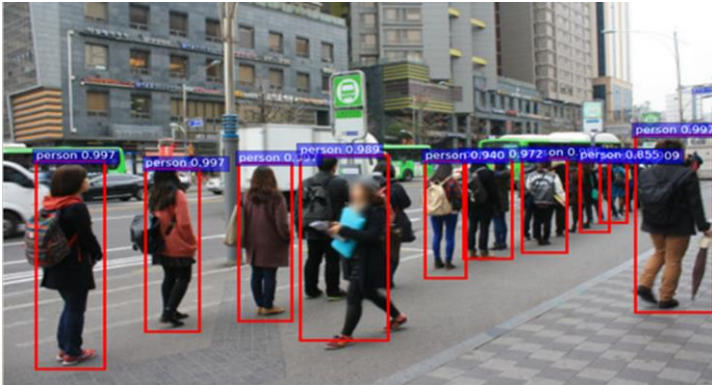


# Dream Chip Technologies ...

- Positioned as a Fabless Microelectronic Engineering Company for medium to large SoC designs covering the whole range from Architecture, Specification, Design, Verification to GDSII
- Technologies: 130nm, 40nm, 28nm, 22nm FDX, 14/16nm FF
- > 70 Employees/ 62 Engineers with 10 ... 20 years SoC design experience
- Based in Hanover (HQ) and Hamburg, Germany
- Member of Silicon Saxony/ Germany
- Cadence Design Center Partner for Tensilica



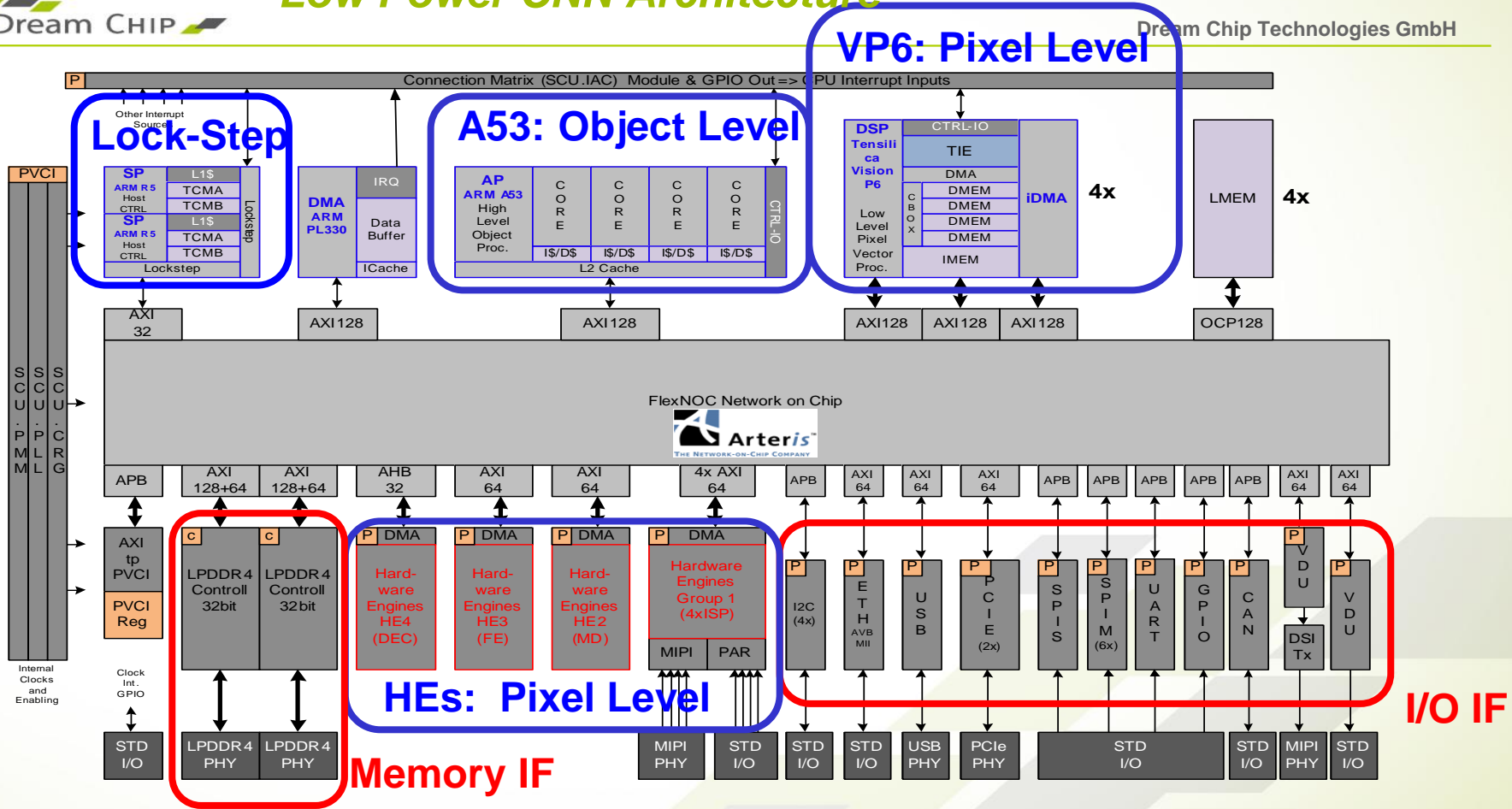
# Target Applications



Typical  
LED  
Flicker

Deflickered  
Sequence

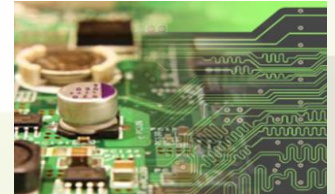
# *MPSoC Chip Architecture*



# *SDIP ASIC Design Flow*

# Verification Concept

## Cadence Incisive Verification Tool Chain





# SDIP Verification Concept

## Cadence Incisive Verification Tool Chain



DVLib

- Chip-level and sub-system verification
- UVM SystemVerilog based verification environments
- Verification environment are configurable to select between usage of
  - IP “simulation models” or
  - IP RTL
- For environments hosting a processor this flexibility allows simulation running real program code or generating “directed” bus transactions.



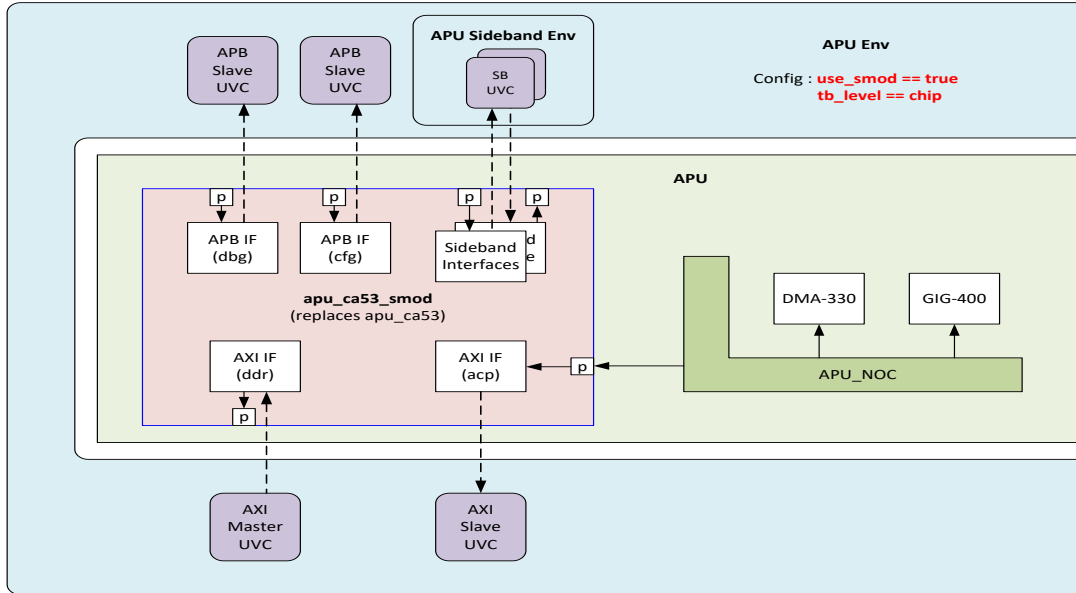
# SDIP Verification Concept

## Cadence Incisive Verification Tool Chain



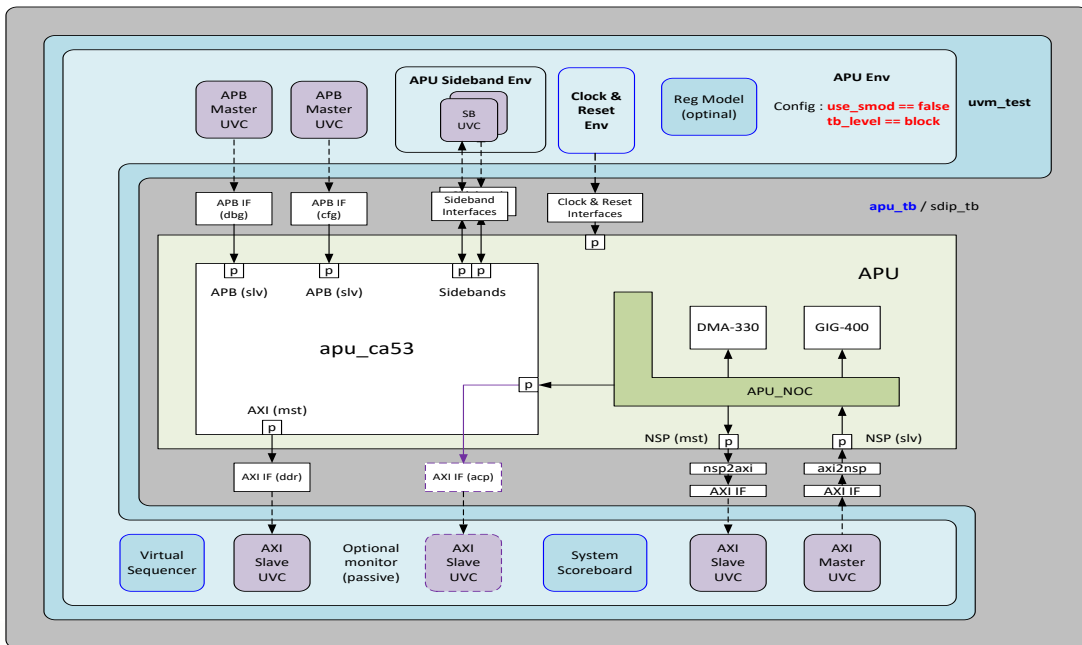
- Sub-system environments available for
  - Application processor unit (APU, including ARM A53)
  - Safety processor unit (SPU, including ARM Cortex R5 lockstep)
  - Digital signal processor unit (DSP, including Xtensa VP6)
  - Memory control unit (DDRC, including DDR controller and PHY model)

# APU Verification Environment (Flavour A)



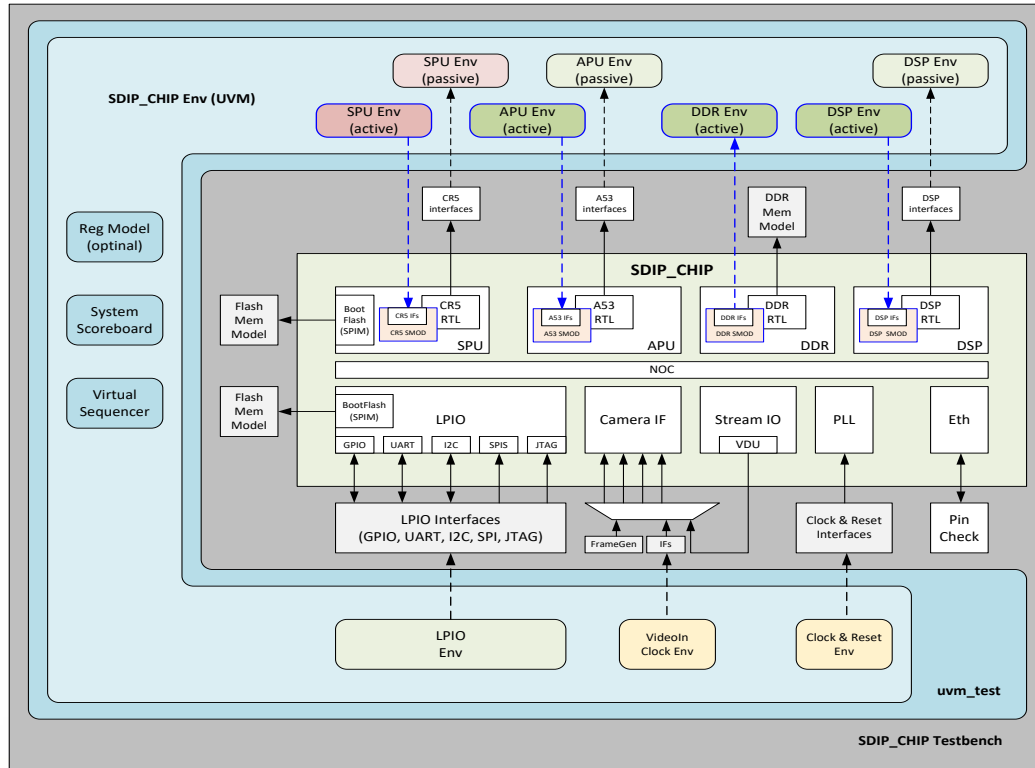
- Environment configured to be used on chip-level using the A53 simulation model
- A53 APB and AXI transfers driven by according UVC sequences
- Remaining sideband port are driven by sideband UVCs

# APU Verification Environment (Flavour B)



- Environment configured to be used on subsystem-level using the A53 RTL
- A53 APB and AXI transfers driven C program code
- Remaining sideband port are driven by IP itself

# SDIP Chip-Level Verification Environment



# Dft and Backend

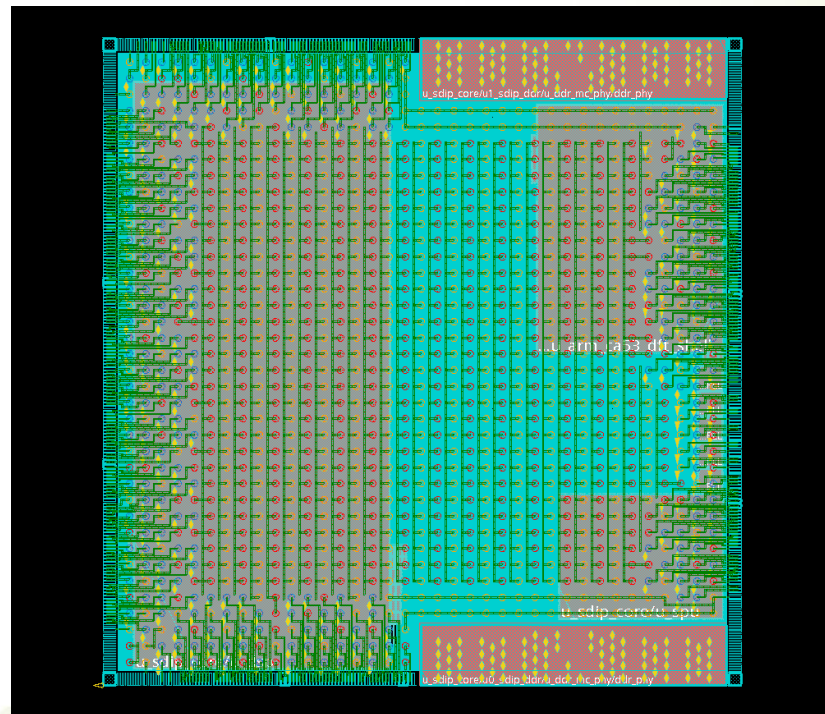
## Cadence Genus/Modus/Innovus Backend Tool Chain



# SDIP Chip: Layout Overview

## Cadence Innovus Backend Tool Chain

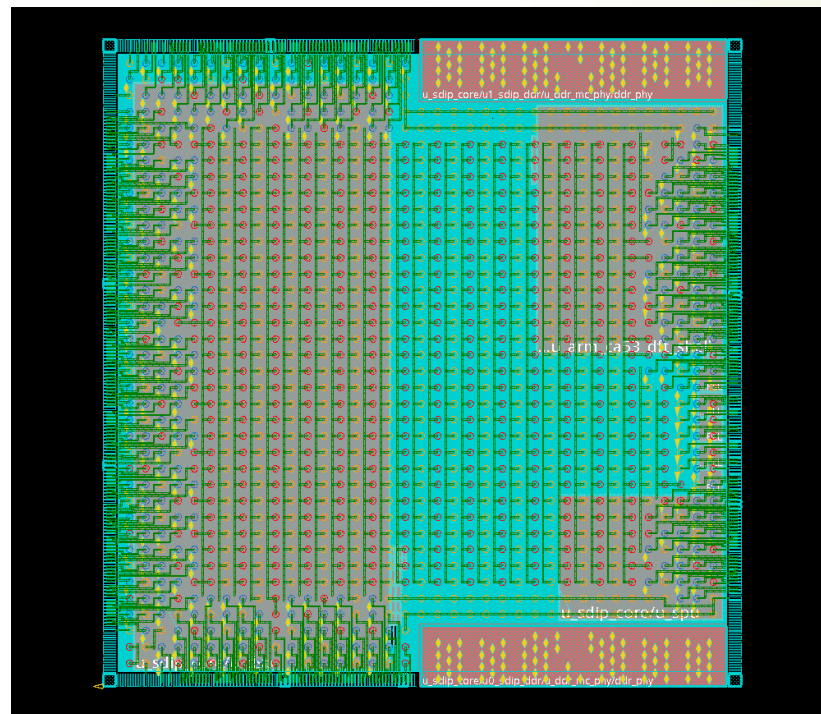
- GF 22FDX technology
- PDK v0.5\_0.1
- 12 track library
- 7885,3 $\mu$ m x 8001,3 $\mu$ m
- 10LM
- Flipchip
  - 1292 bumps
  - 405 signal IOs
  - 150 $\mu$ m/200 $\mu$ m pitch
- LVT/SLVT + FBB
- up to 1 GHz
- 0.8V core / 1.8V IO



# SDIP Chip: Design Info

## Cadence Innovus Backend Tool Chain

- ~15.6M Instances
- ~11.6mm<sup>2</sup> RAM
  - 489 insts / 7426 kBytes
  - only 9 different RAM cells
- Prepared for FBB
- Timing Optimization
  - One SDC only
  - 4 setup analysis views
  - 9 hold analysis views



LPDDR0

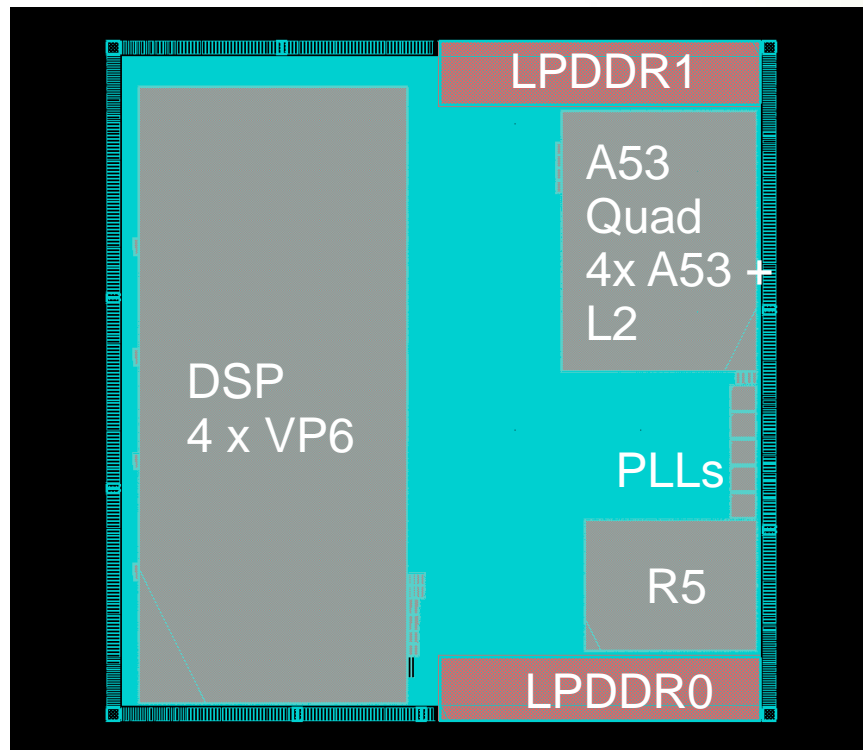


# SDIP Chip: Hierarchical Layout with Innovus

## Cadence Innovus Backend Tool Chain

sdip\_chip

- ARM A53
  - 4 x A53 CPU
- ARM R5
- DSP
  - 4 x Tensilica VP6
- 2 x 32bit LPDDR4
- 5 x PLL



# Layout Runtime Info

## Cadence Innovus Backend Tool Chain

- A53 CPU 12h
- A53 Quad 12h
- VP6 60h
- DSP 30h
- R5 lockstep 17h
- SDIP chip 70h
- total 160h
- 3 x Intel(R) Xeon(R) CPU E5-2643 v2 @ 3.50GHz (12 Cores / 256GB RAM)
- 5 x Intel(R) Core(TM) i7-6700K CPU @ 4.00GHz (8 Cores / 128GB RAM)
- multiple "small" machines
- organized as SunGridEngine

# Static Timing Analyses

## Cadence Tempus

- Hierarchical Approach
  - A53 Quad
  - DSP
  - R5 lockstep
  - SDIP chip
- 34 Scenarios
- 6h runtime / 4 DMMC Jobs  
(8 CPUs each)



# Layout Verification

## 3<sup>rd</sup> Party Toolchain

- Cadence PVS was not qualified for signoff at TO time
- Hierarchical Approach not possible for sign-off
- high run time
  - DRC 72h (3 x 12 CPUs / > 1TB RAM)
  - LVS 3h
  - FILL 89h (runset not prepared for massive parallel computing)



# Power Analyses

- Heavy computing on one A53 at 500MHz adds +90mW P(core)
- Each additional heavy computing A53 at 500MHz core adds +25mW P(core)
- Heavy computing on VP6 RISC at 500MHz adds +290mW P(core)
- Heavy computing on VP6 SIMD at 500MHz adds +975mW P(core)
  
- A53/VP6 RISC computing: Mersenne Twister pseudo-random number generator
- VP6 SIMD computing: Vector multiplication

- One LPDDR at 1066MHz adds **+715mW P(total)**
- Second LPDDR at 1066MHz adds **+300mW P(total)**
- Using LPDDR at 1333MHz adds **+150mW P(total)** per controller

- Multiview application runs at **+300mW P(total)**, **+190mW P(core)**
- Topview application runs at **+450mW P(total)**, **+350mW P(core)**
- Topview computing consumes **165mW P(core)**



# SDIP ES 3.0 -> 2018

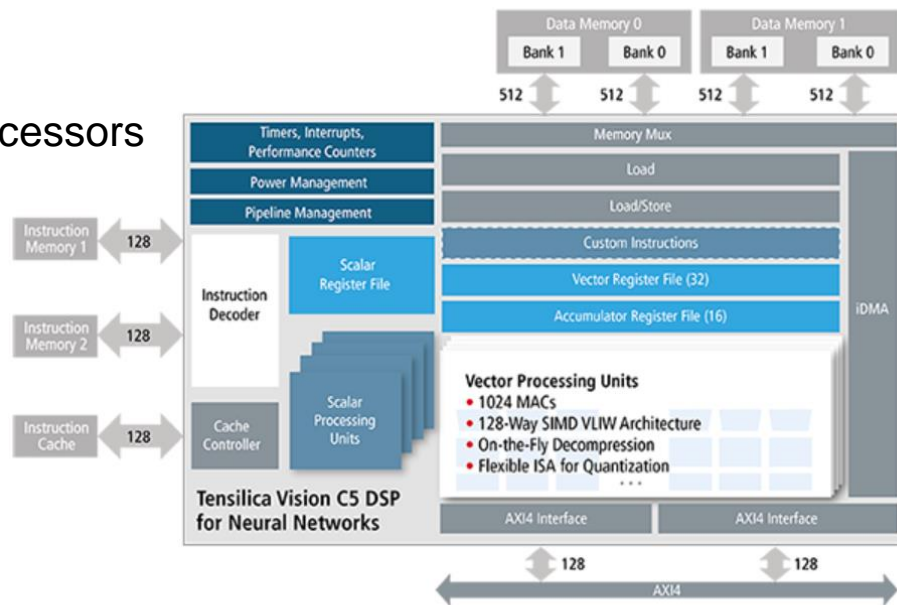
# Roadmap / Technology Improvements

- GF 22 nm FDSOI PDK 1.2
  - better PPA
  - use 8-track libraries
  - fix DDR phy weaknesses
- Power Management Optimization
  - restrict use of LVDS cells
- Flow
  - use new Cadence LBIST flow
  - use Cadence PVS for DRC / LVS sign-off
  - use hierarchical sign-off and fill flow



# Roadmap / Features

- Replace two Vision P6 by Vision C5 Processors
- Add USB interface
- Add 2D GPU
- Minor bug fixes / improvements



Vision C5 DSP for Neural Networks Block Diagram

# Demos



accelerates your product



### ASIC and FPGA SoC D

- Automotive, industrial and consumer
- Complete turnkey solutions – e.g. ARM based
- ASIC even for low volumes
- Programmable processors – Tensilica



### Video and Image Processing

- Full ISP pipeline
- Customized image algorithms – e.g. object detection
- Video pre- and post-processing
- Audio and video code development



### Embedded Software Development

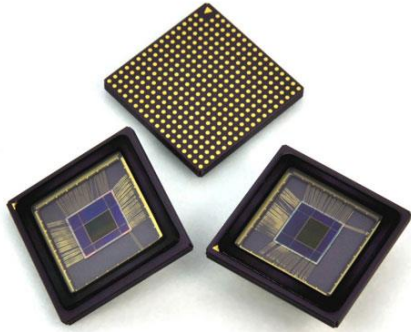
- Linux drivers and applications
- Android system programming
- Software defined radio



### System and Prototype Design

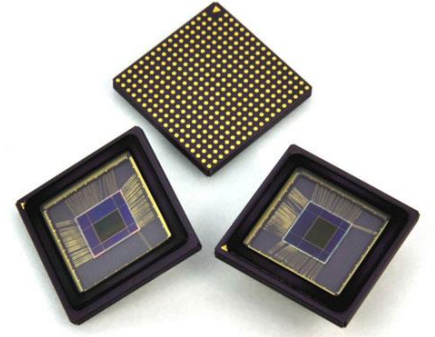
design and layout





# Thank You!

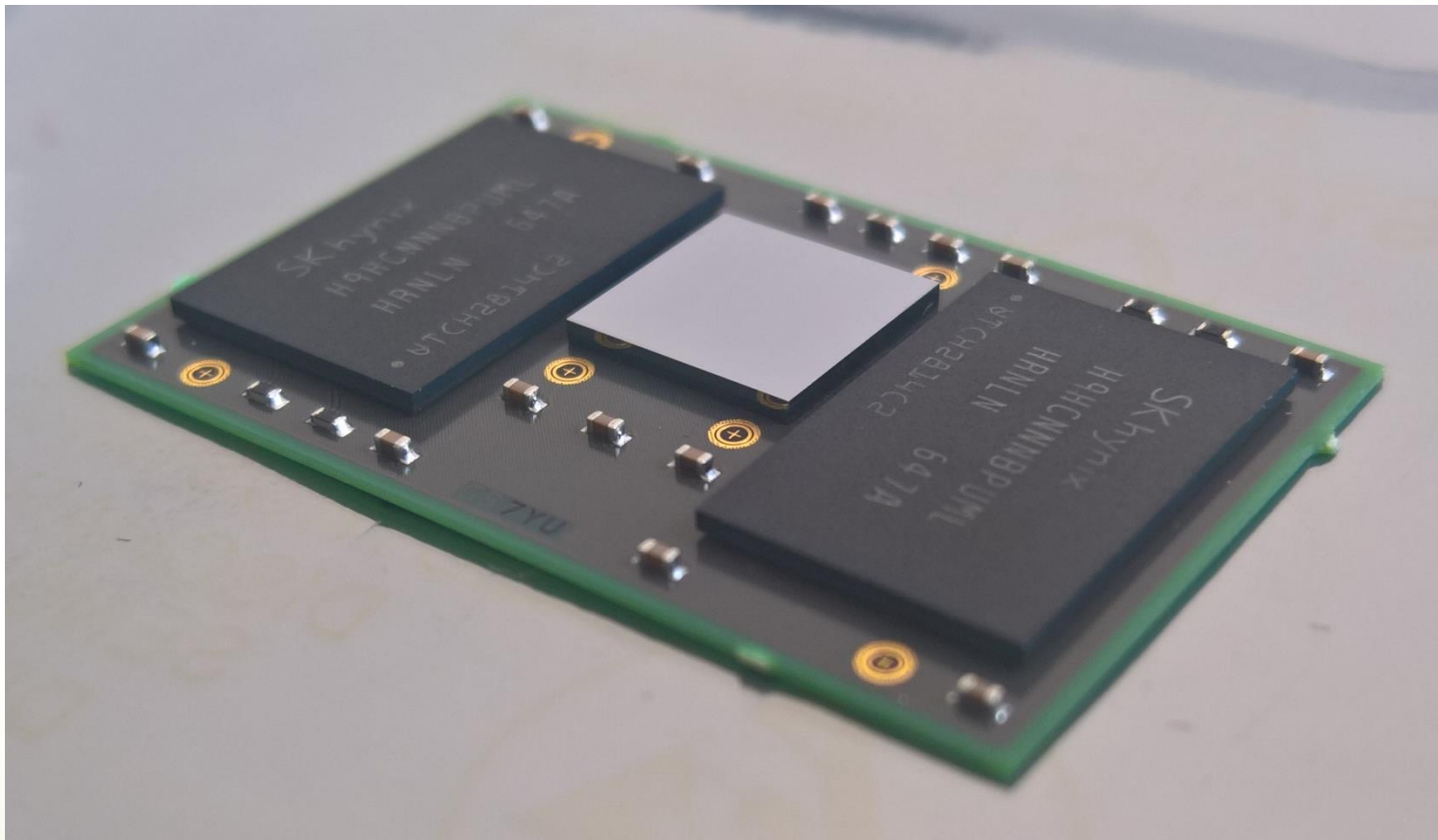
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# *MPSoC Chip / Starter Kit*



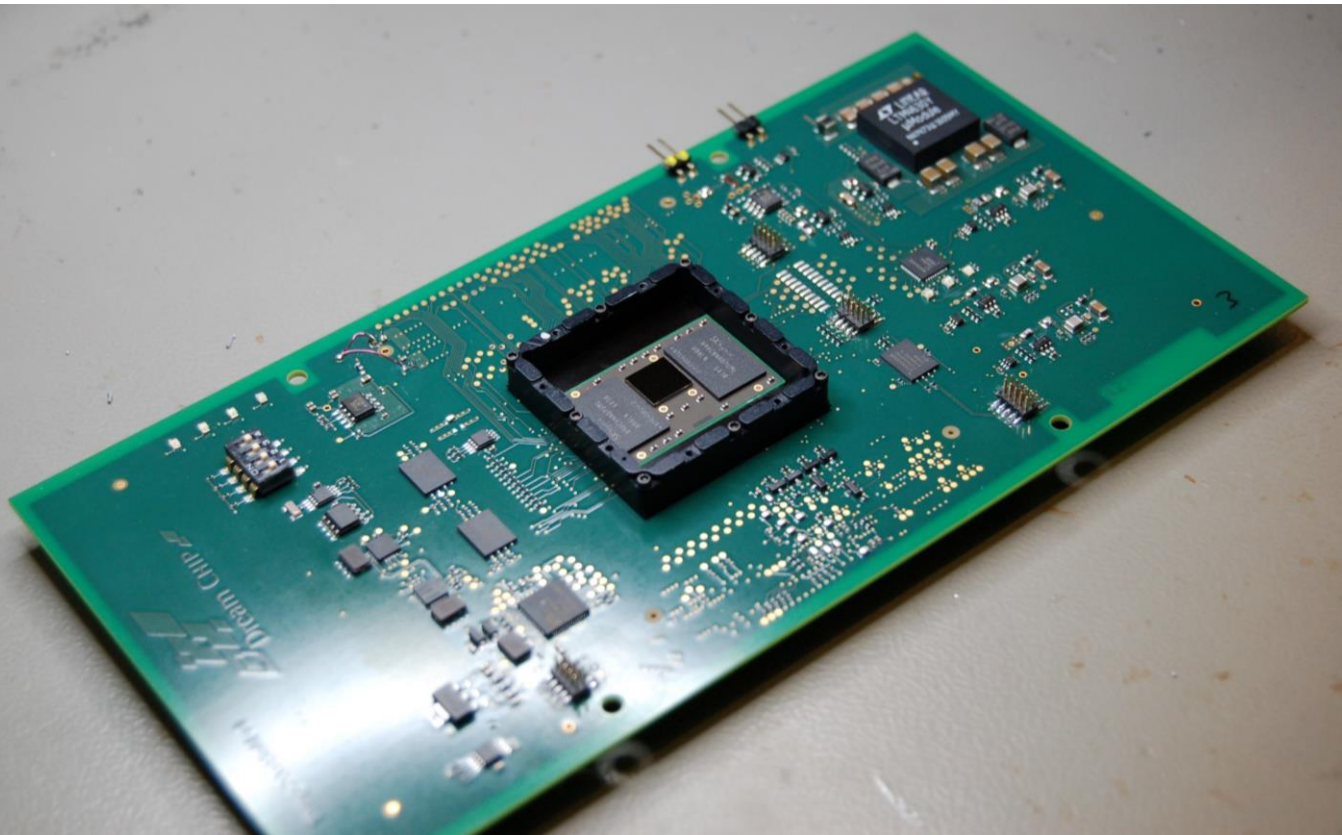


### System-on-Module features

- 4GB LP-DDR4 3200 RAM

### Interfaces

- Four 300MB/s video inputs
- One 300MB/s video output
- Gigabit Ethernet



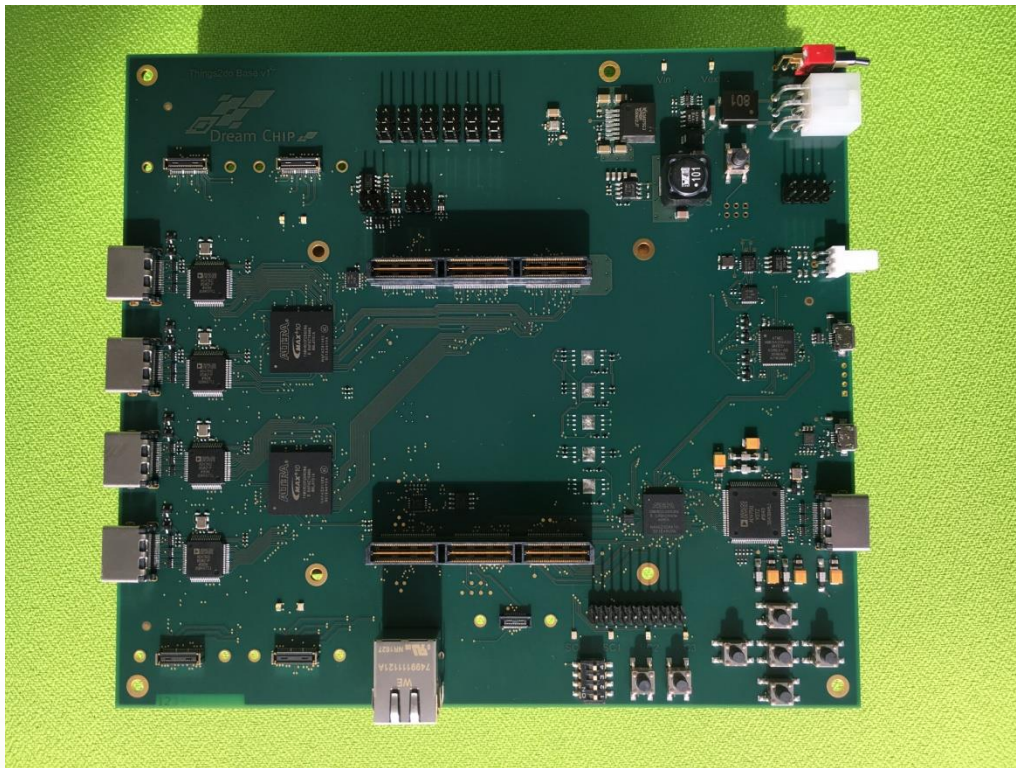
## Overview

- Power management and measurement
- Chip power supplies included

## Benefits

- Reduced application-specific baseboard complexity
- Interfaces customizable to application requirements

## 4xHDMI Application Board



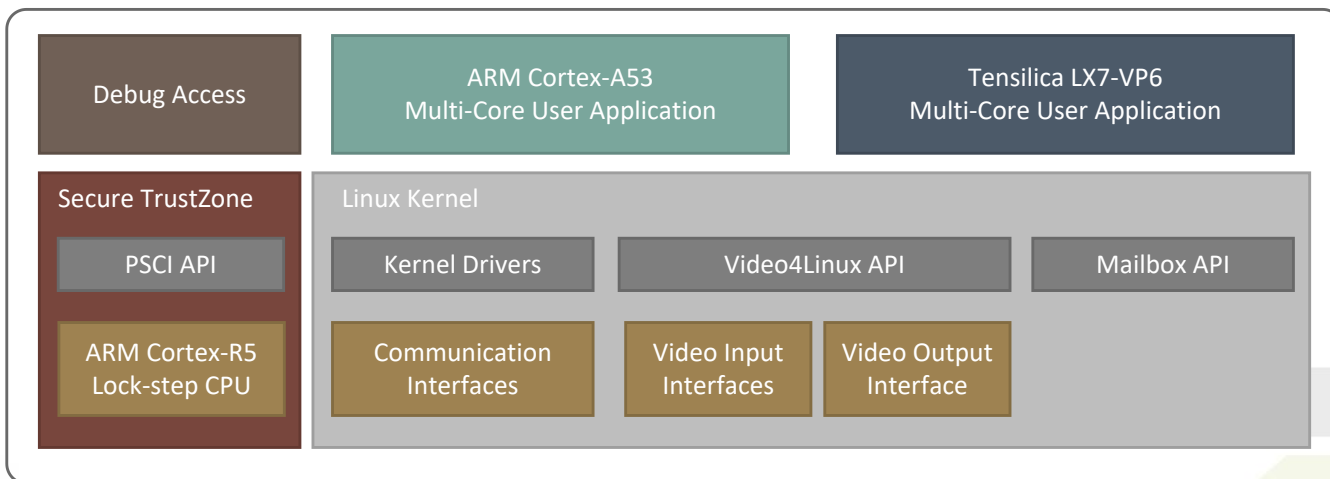
### Overview

- DCT ADAS Quad-HDMI Base Board
- Four HDMI 1.4b inputs
- One HDMI 1.4 output
- Custom high-speed headers available

### Base board features

- Video data rates up to 1080p60
- Two Intel MAX10 10M08DC FPGAs
- Four high-speed interface headers
- Video input synchronization
- True output genlock possible

# Software Development Kit



## Overview

- DCT ADAS Software Development Kit
- LEDE distribution with stable Linux 4.4.42
- 32-bit and 64-bit flavors available
- Tensilica LX7-IVP6 development support
- Kernel API drivers

## SDK features

- video framework
- Tensilica LX7-VP6 support