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MD, COO Dream Chip

**SmartHeaP – A 22nm FDX Ultra Low Power Design
based on Cadence Tensilica Processor Architecture for
Hearing Aid Applications**

Tensilica Day, LUH IMS Hanover, Feb. 7th, 2018



SmartHeap – Project Intro

- BMBF call “New electronic systems for intelligent medical technologies (Smart Health)” managed by VDI/VDE-IT
- Previous Projects as part of the excellence cluster Hearing4All

- Project Start: April 2018



GLOBAL
FOUNDRIES



- Duration: 3 years **cadence**[®]

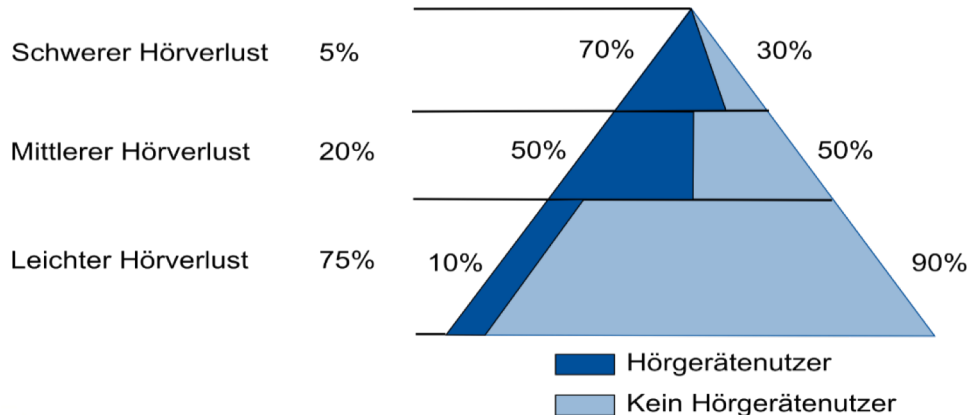


- Participants: Cadence, Catena, Dream Chip Technologies, Global Foundries, Fraunhofer IIS, Hoertech, Leibniz University Hannover (IMS, Prof. Blume)



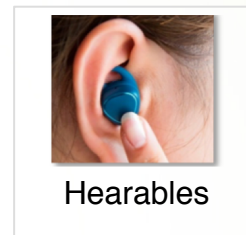
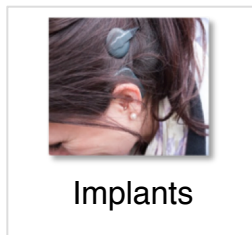
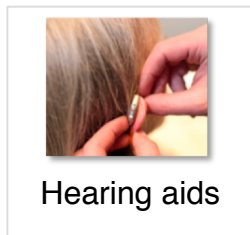
Project Motivation

- Today 360 Mio. people suffer from hearing loss (that's 5.3% of the worlds population, 9% of the kids)
- Almost 30% of elder people (>65 yrs) have a hearing loss



- Tremendous limitation of the participation in the social live
- Growing number of hearing aids users (by +30% over the last 4 years)

Hearing Aids – Applications and Markets



Soren Nielsen,
William Demant, 2015

There is just single source hearing aid processor available as IP!

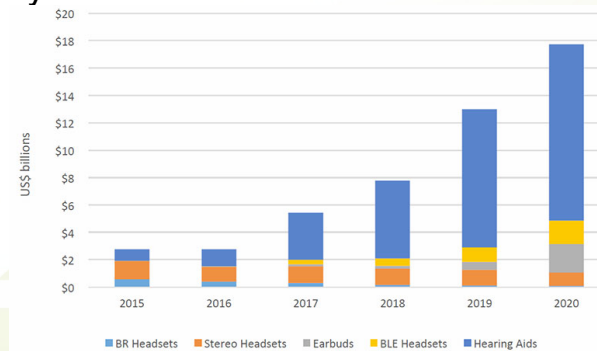
By today, non of the available DSPs is C programmable!

Time to market for new algorithms is very critical!

2016:

- 1,24 Mio. p.a. hearing aids sold in Germany
- 1,42 Bill. € revenue. p.a. in Germany

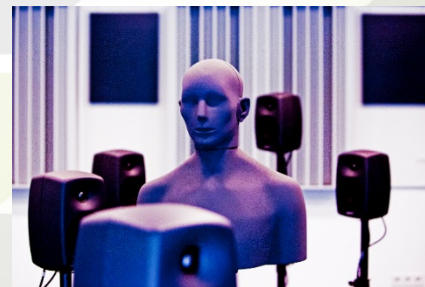
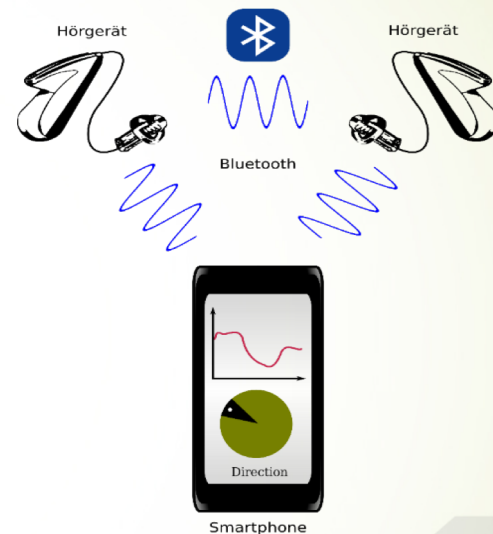
2020:





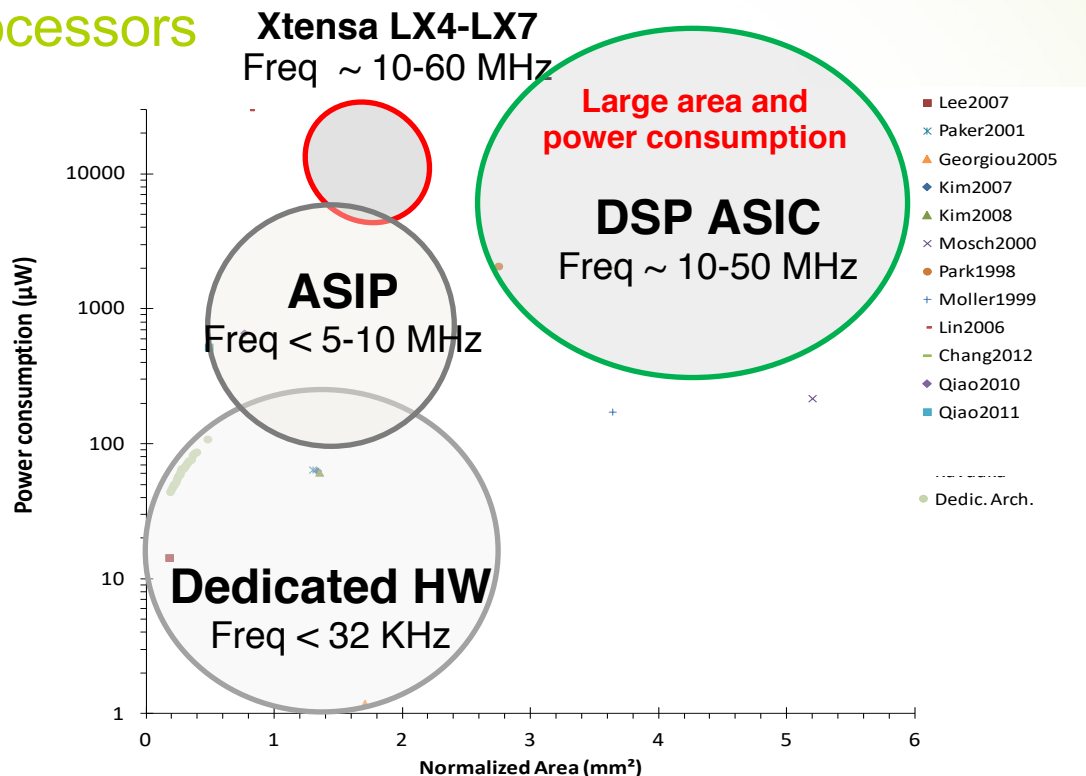
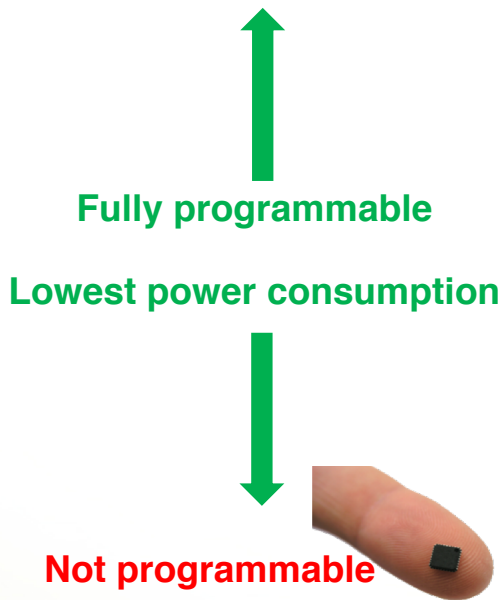
SmartHeap Algorithmic Innovations (Hörtech)

- Improved fitting for hearing aids using binaural broadband signals
→ Solution: Novel binaural, bandwidth-dependent dynamic compressor (Oetting et al, 2015)
- Reduced speech intelligibility in everyday listening situations
→ Solution: Binaural localization of the target speech source (Adiloğlu et al, 2016)
- Better speech understanding in noisy environments
→ Solution: Binaural noise reduction (Gerkmann et al)



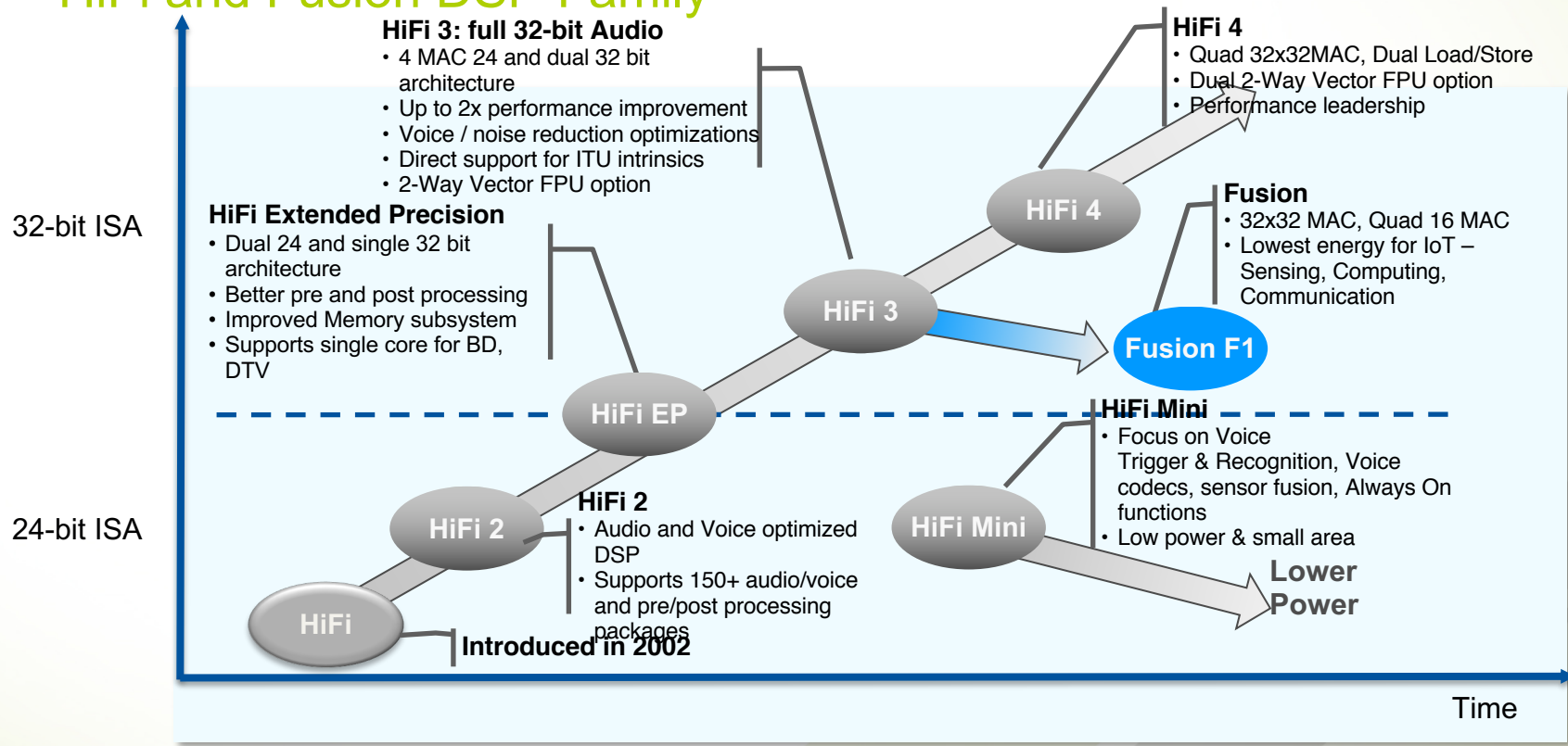


Hearing Aids Processors



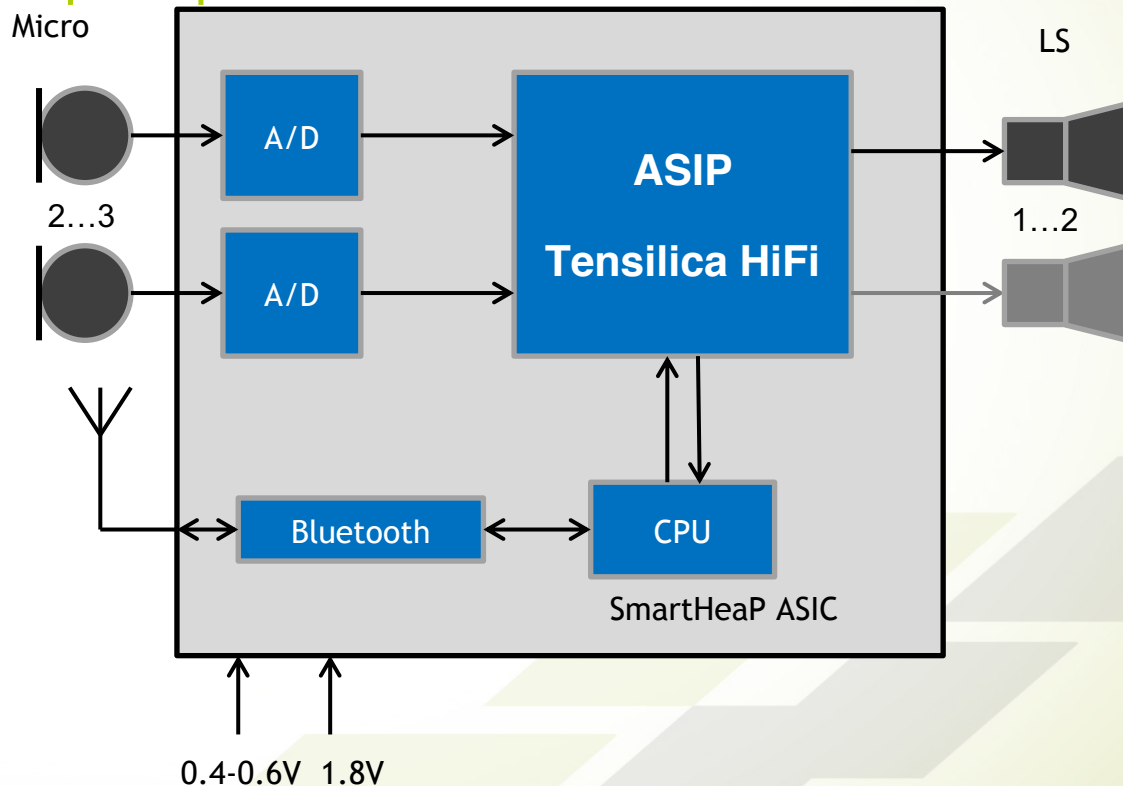


HiFi and Fusion DSP Family



Block Diagram SmartHeap Chip

- Technology: 22nm FDX
- A/D: 18-20 bit@32kHz (>90dB)
- Tensilica HiFi3 with modified ISA
- Bluetooth LE for smartphone connectivity integrated
- Ultra low power design based 0.4 V libs





Work Packages

System-Level Design

- Algorithmic Design
- Mapping to SW/HW Blocks
- Technology Selection
- Power Simulation
- Performance and Area Estimation



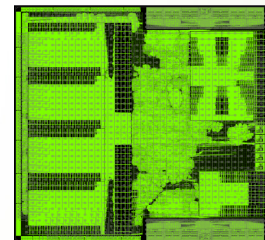
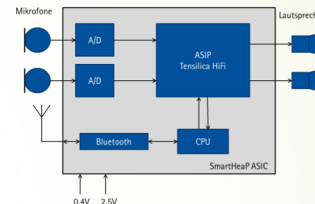
RTL Design

- RTL Design
- IP Selection
- Power Optimization
- Verification

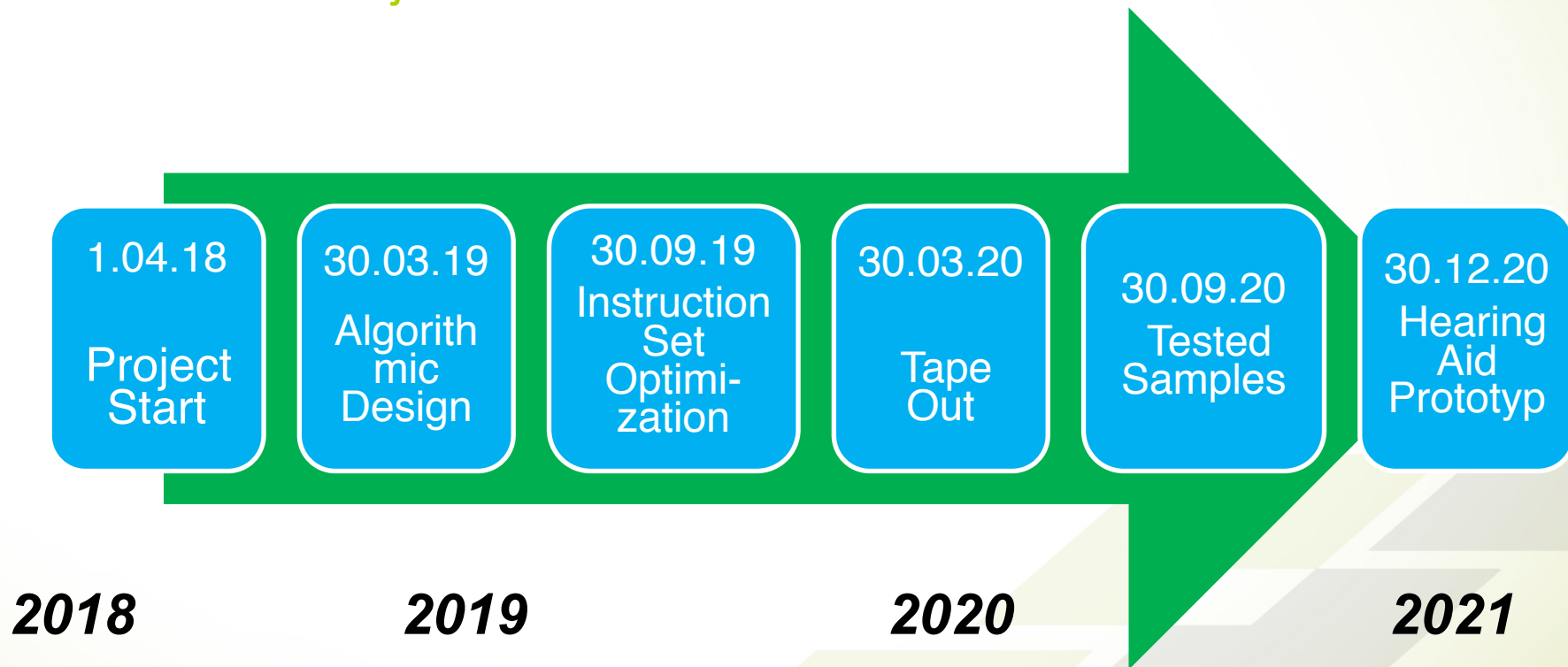


Implementation

- Synthesis to Gate Level
- Floorplan, Place&Route
- Further Power Optimization
- Package Design
- Prototype Design

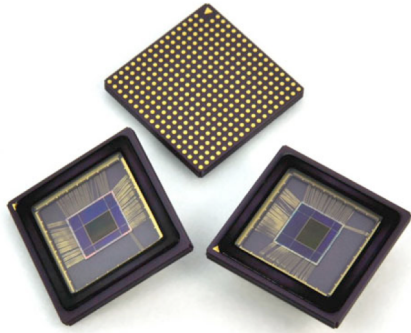


SmartHeaP Project Schedule

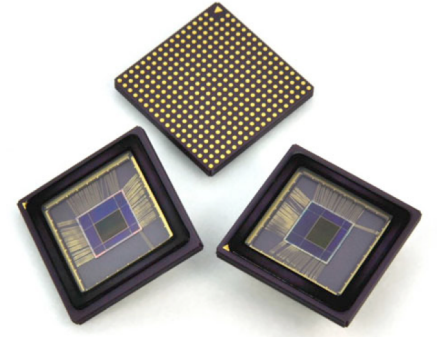


SmartHeaP Partners





Thank You!



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