Novel FPGA-Architecture

Technical Features FPGA

(Field Programmable Gate Array)

Cologne Chip

- Configurable digital circuit
- Function is not defined during the manufacturing process, but through configuration.
- Unlike a microprocessor, not program-controlled
- Any logical (boolean) functions can be configured
- Circuit elements are connected by configurable routing connections
- Very fast, as non clocked circuits can be realized as well
- Fast Time to Market
- More difficult to copy than conventional circuits
- Changes to existing hardware possible by loading new configuration
- Realizes function of an ASIC (Application Specific Integrated Circuit) without Mask costs and additional production time

Novel architecture of the Cologne Chip FPGA

- Double checkerboard architecture:
  - There are only switch boxes on every second field
  - Big and small switchboxes alternate
- Extremely small LUTs (Look UpTable)
- Complex Configurable Element (CPE) with the following properties:
  - 8 combinatorial inputs with 7 LUT2
  - 2 flip-flops or latches
  - 2 routed outputs, 2 outputs for additional functions
  - 2 cascaded, not routed connections in the X and Y directions
  - very flexible clock routing, plus 4 global clocks
  - CPE can be configured with 2x 4 inputs or 1x 8 inputs
  - CPE can be 2-bit full-adder or 2x2 multiplier
- Configuration memory of 8-bit latches leads to low internal routing and low SEU propabiity.
- 12 routing layers simplifys Place & Route software.
- Direction Change Multiplexer allows direction change of a signal in every switchbox

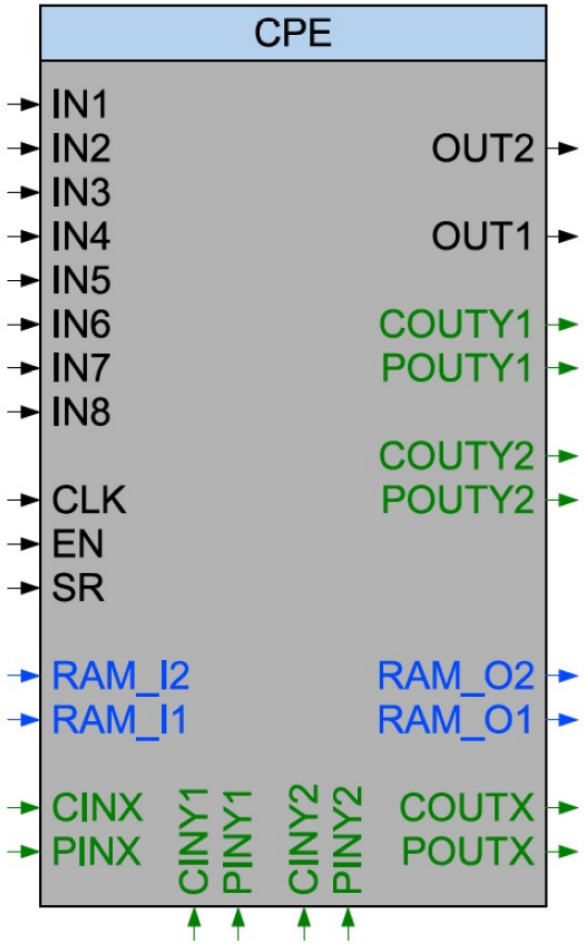
Commercial Situation in the FPGA world market

- 2 large and 2 smaller companies
- All US-based
- Almost all analysts expect the market to continue to grow strongly.
- Companies (revenue and EBIT 2018 in million $US in the FPGA segment):

XILINX:	Sales: 2,540, EBIT: 750	
Intel PSG (formerly Altera):	Sales: 2,100, EBIT: 500	
MicroChip (form. Microsemi,Actel):	Sales: 200, EBIT: 40	(estimated)
Lattice:	Sales: 200, EBIT: -50	(estimated)

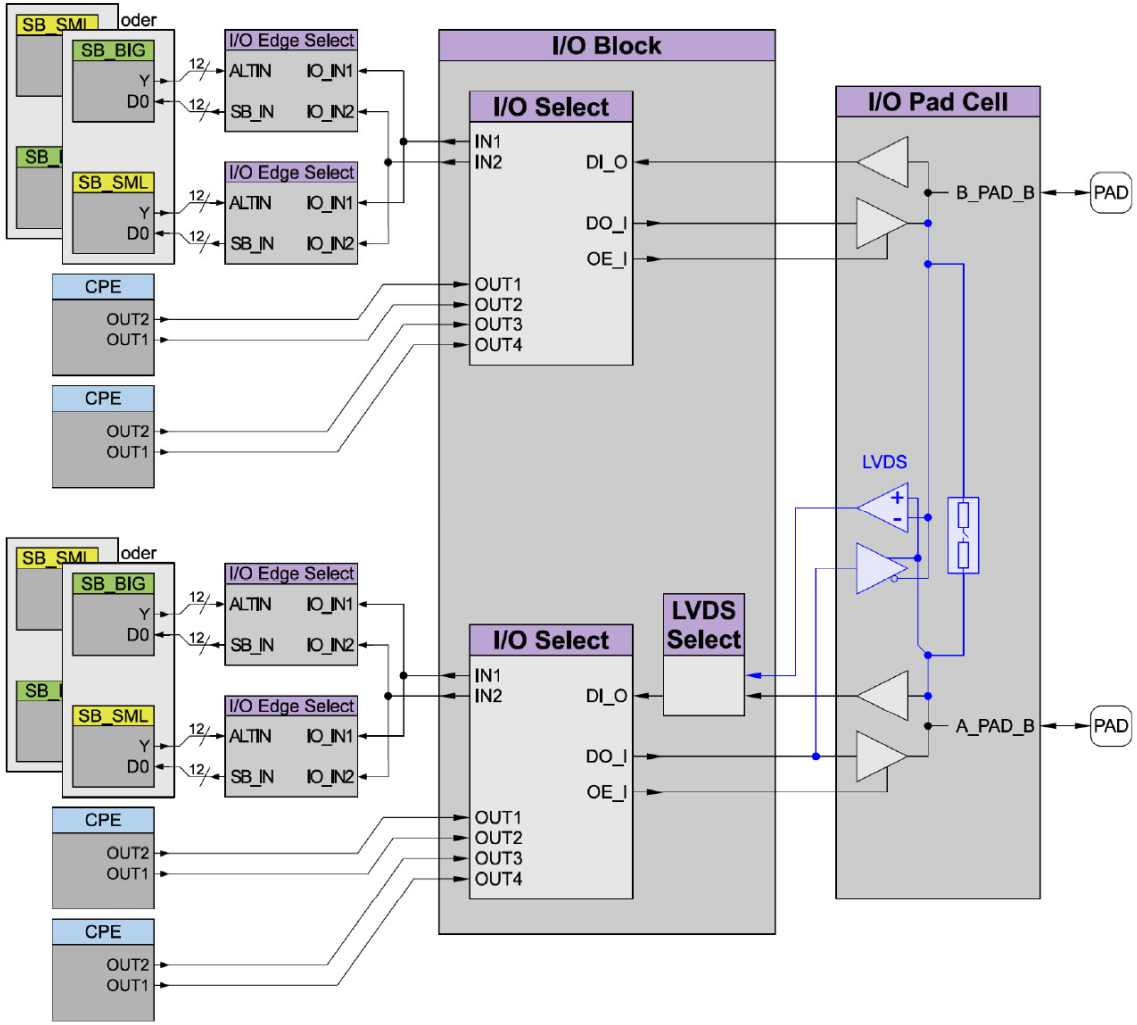
- So the world market is about $US 5 billion.
- With the exception of Lattice, all FPGA manufacturers earn approx. 30% EBIT.
- Even with market shares in the lower single-digit percentage range, Cologne Chip has very attractive commercial opportunities. There are also special Market entry advantages as the only manufacturer in Europe and also "Made in Europe".

Central Programmable Element (CPE)



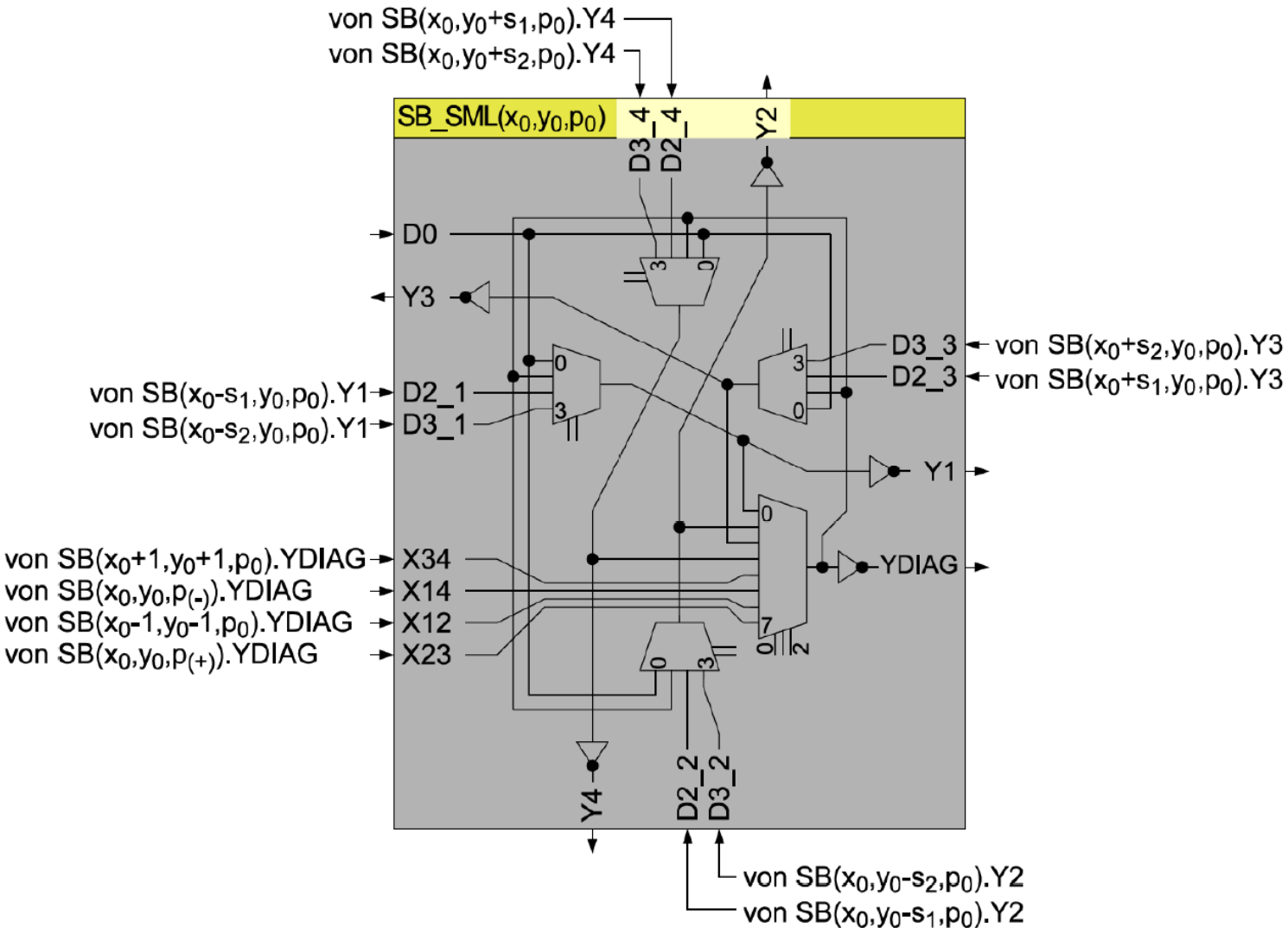
Signals of a CPE (fixed connections in green, RAM-connections in blue)

I/O Block as Interface to chip outside

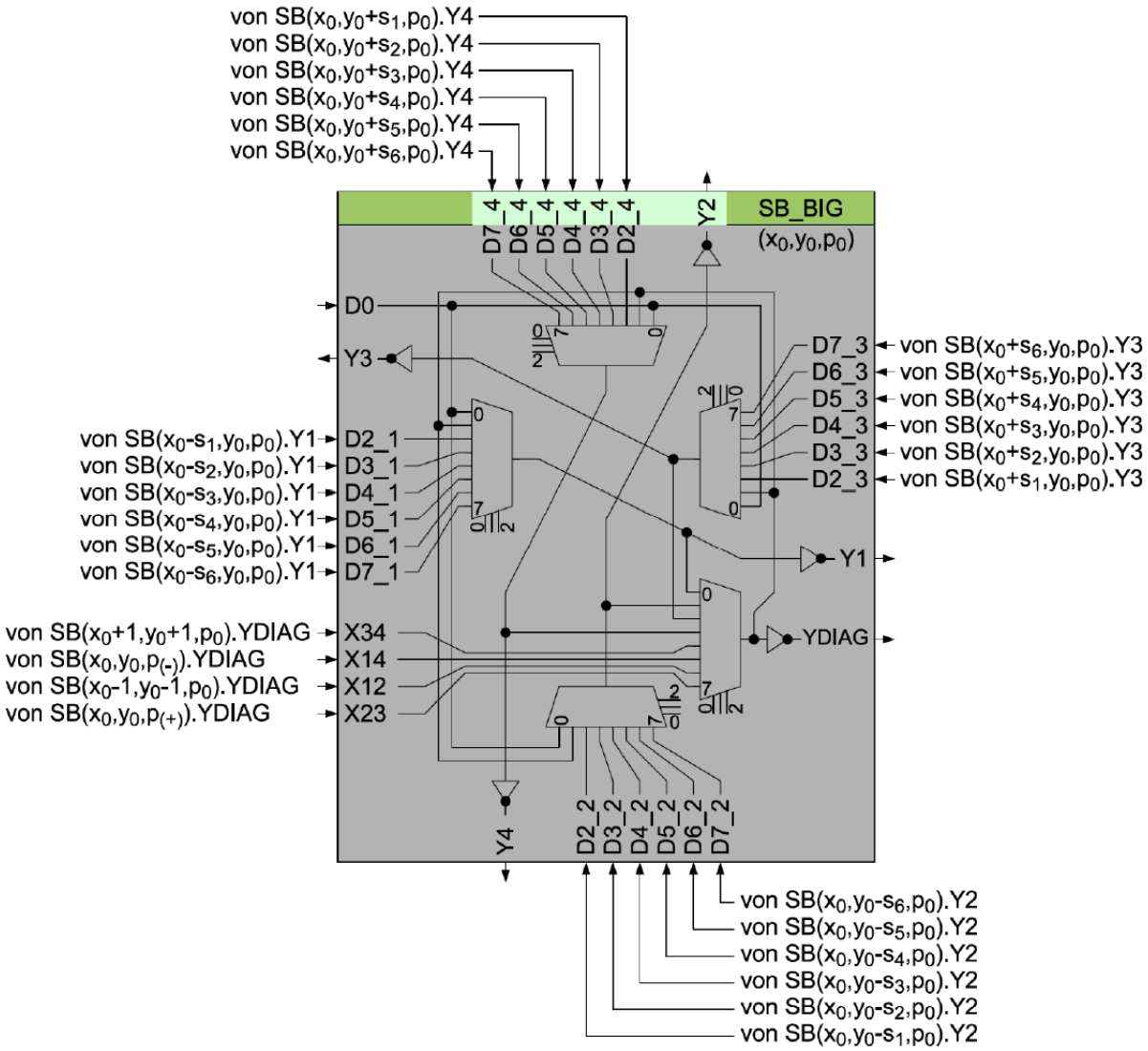


Simplified circuit diagram of I/O block

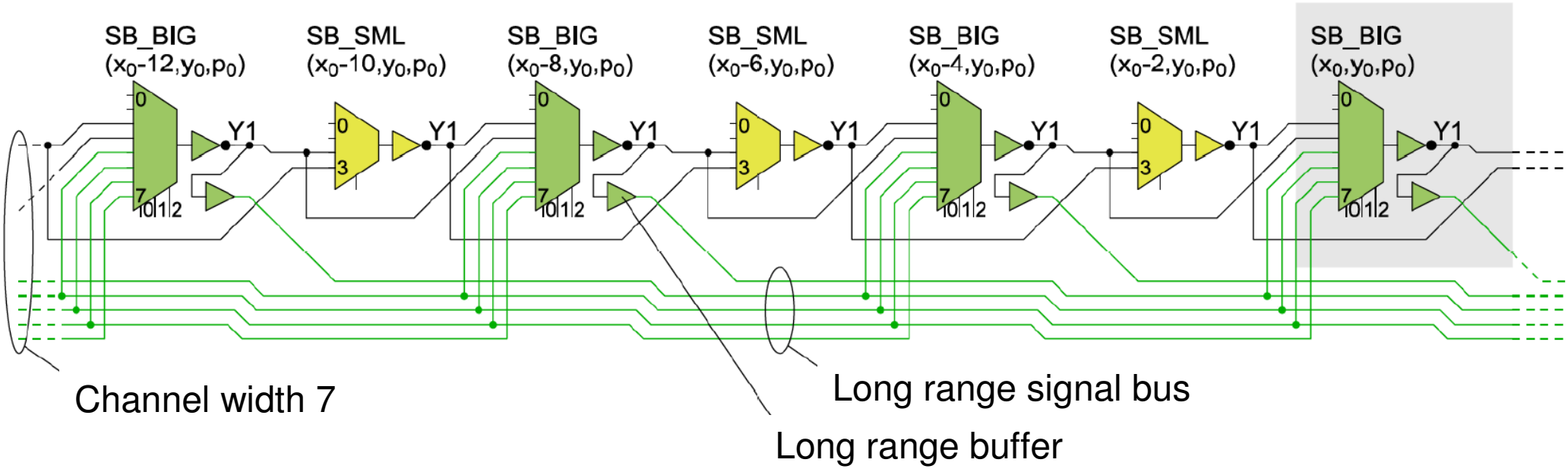
Switchbox (small) for Routing



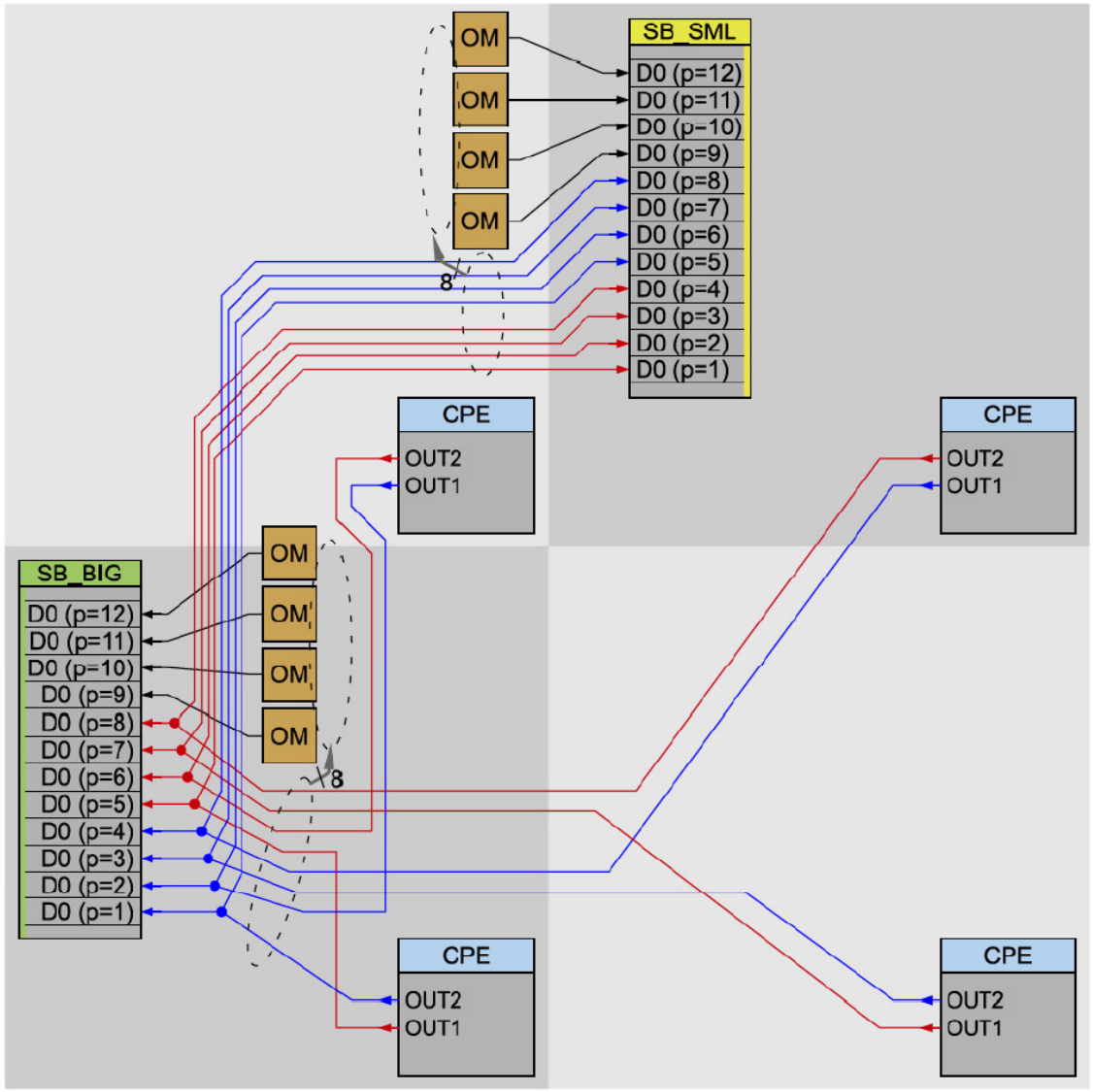
Switchbox (big) for Routing



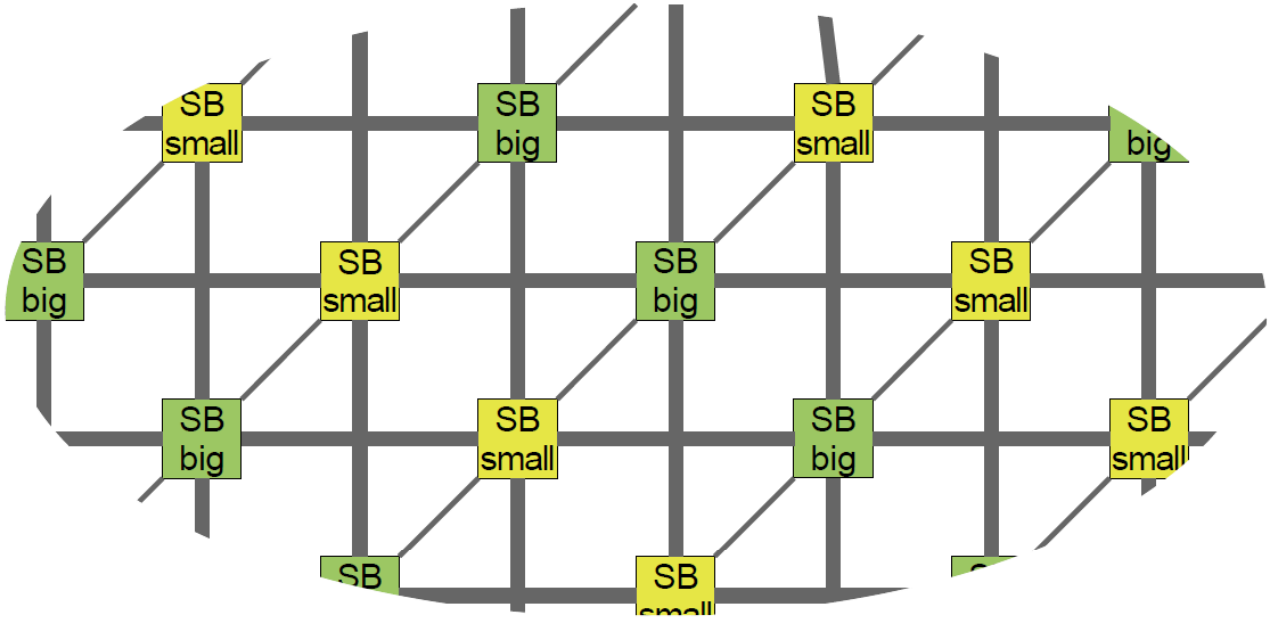
Switchbox-Routing in one dimension

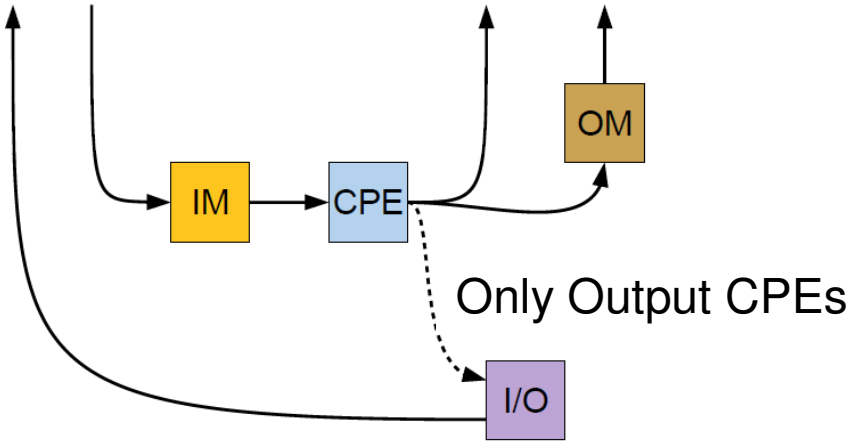


Interconnections of CPEs with Switchboxes



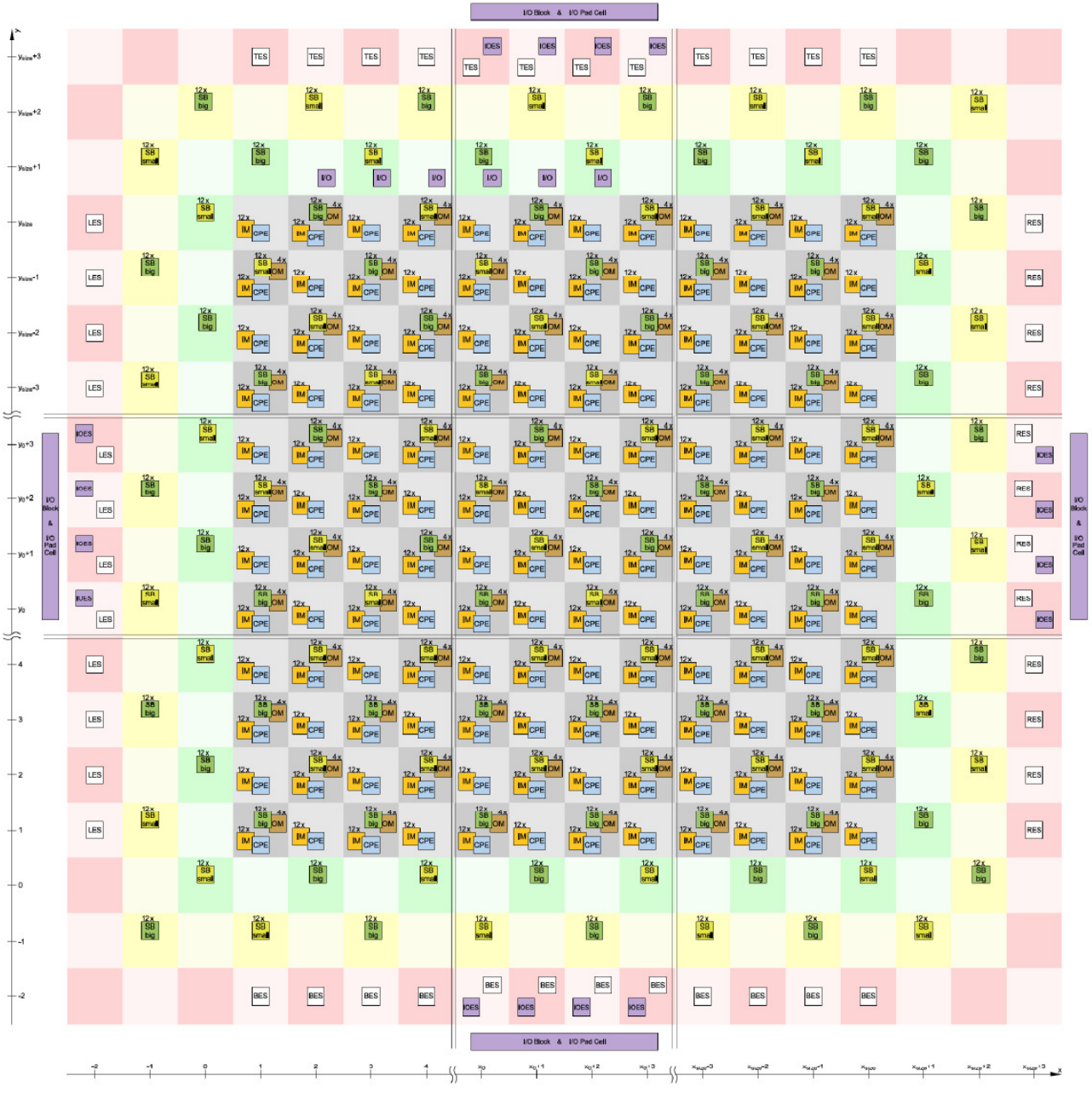
Interconnections of FPGA Circuit Elements



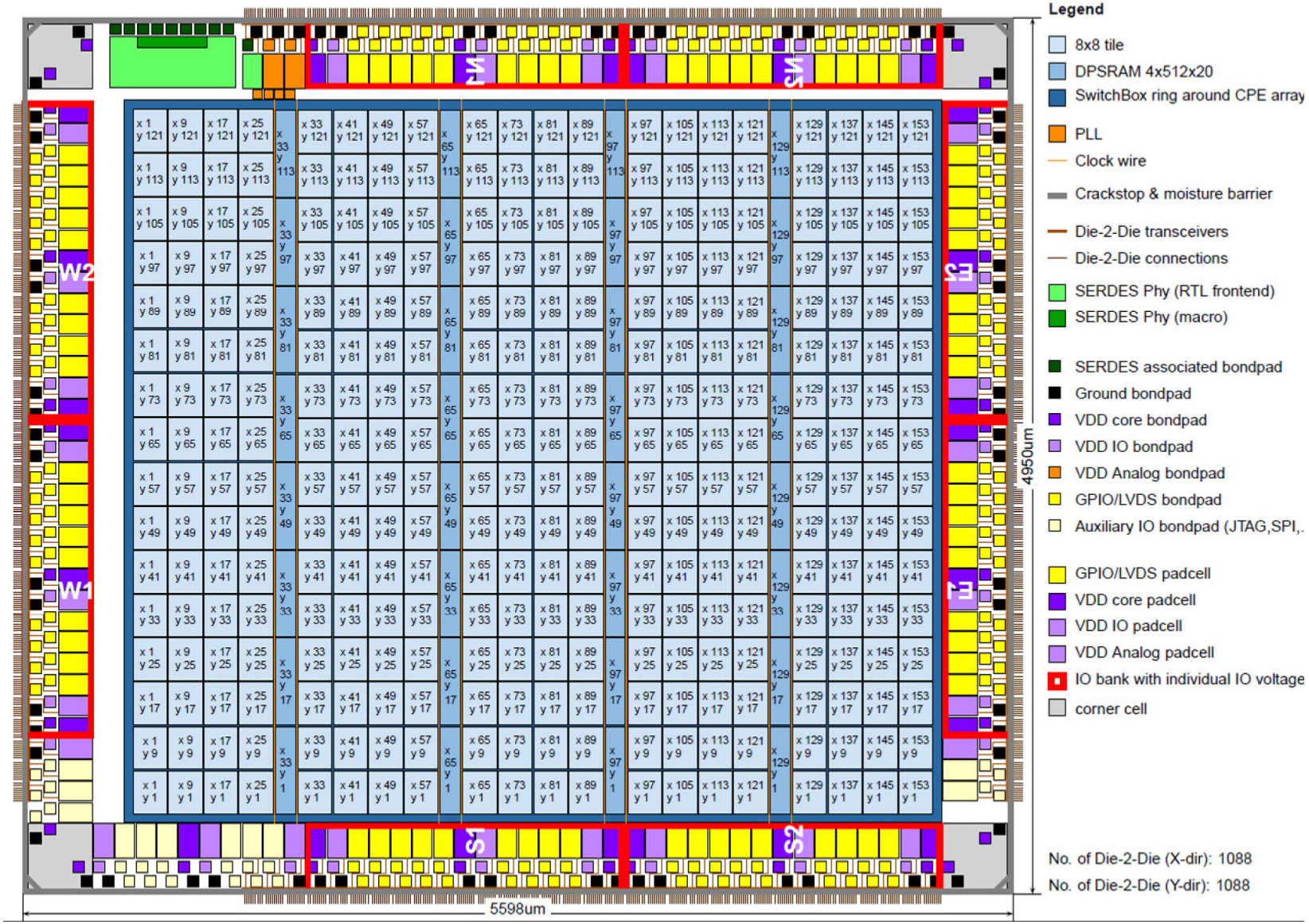


Overview: Strukture of the FPGA

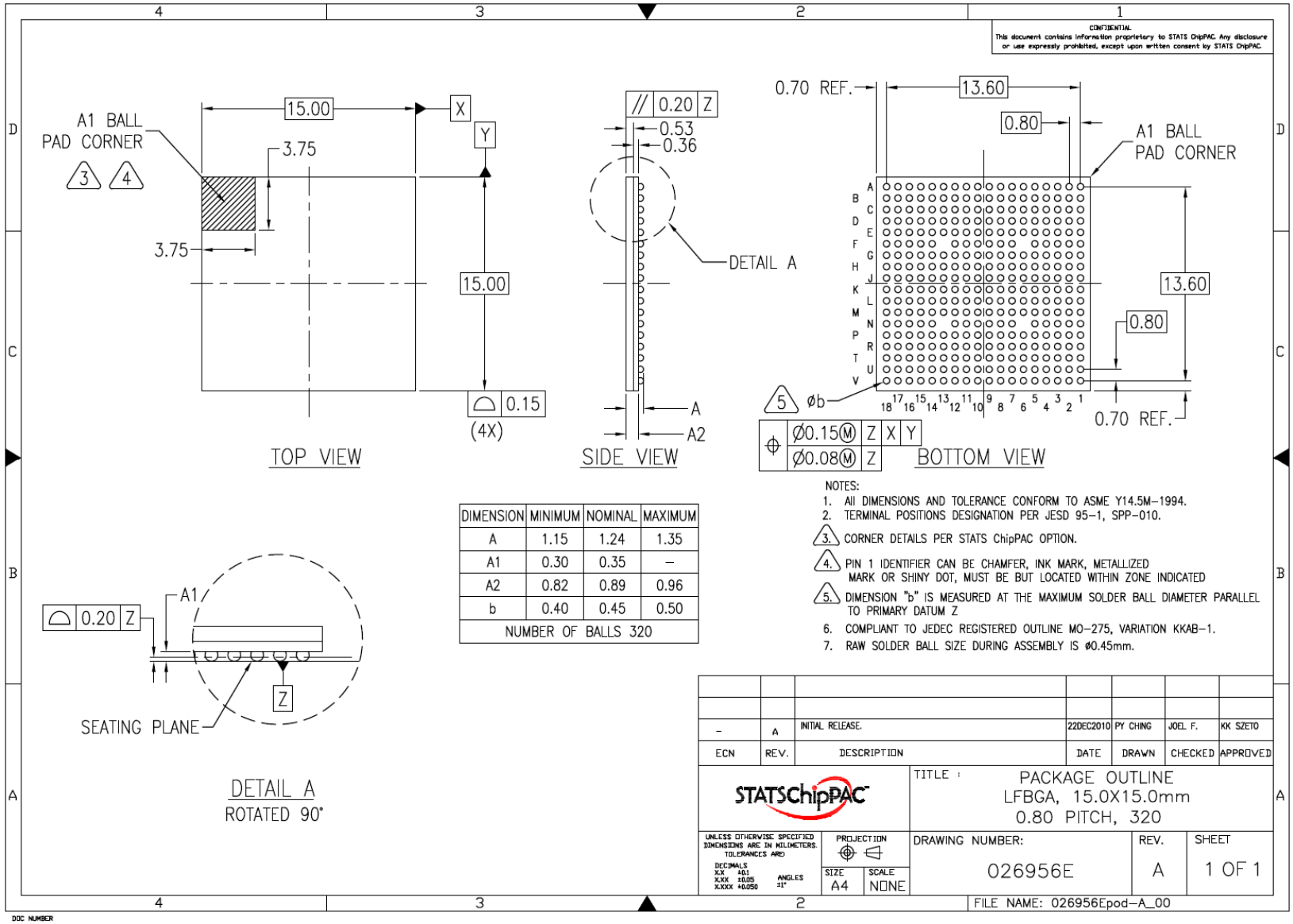
Cologne Chip



Overall View of the FPGA Die



Package of the FPGA: 320 ball LFBGA



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	1.15	1.24	1.35
A1	0.30	0.35	–
A2	0.82	0.89	0.96
b	0.40	0.45	0.50
NUMBER OF BALLS 320			

NOTES:
1. All dimensions and tolerance conform to ASME Y14.5M–1994.
2. Terminal positions designation per JESD 95–1, SPP–010.
3. Corner details per STATS ChipPAC option.
4. Pin 1 identifier can be chamfer, ink mark, metallized mark or shiny dot, must be but located within zone indicated
5. Dimension "b" is measured at the maximum solder ball diameter parallel to primary datum Z
6. Compliant to JEDEC registered outline MO–275, variation KKAB–1.
7. Raw solder ball size during assembly is ø0.45mm.

ECN	REV.	DESCRIPTION	DATE	DRAWN	CHECKED	APPROVED
–	A	INITIAL RELEASE.	22DEC2010	PY CHING	JOEL F.	KK SZETO

STATSChipPAC

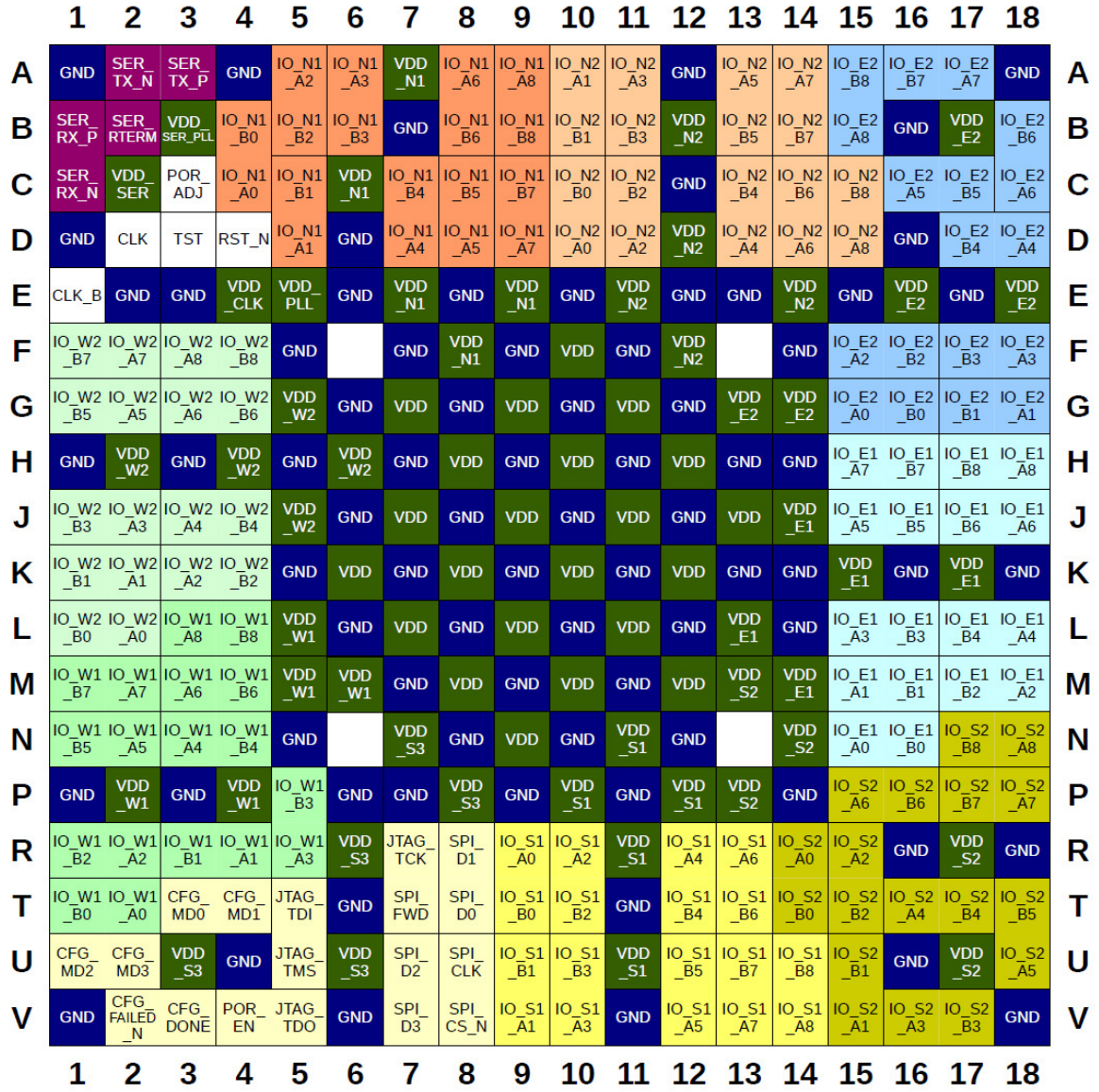
TITLE : PACKAGE OUTLINE LFBGA, 15.0X15.0mm 0.80 PITCH, 320

DRAWING NUMBER: 026956E | REV. A | SHEET 1 OF 1

SIZE A4 | SCALE NONE

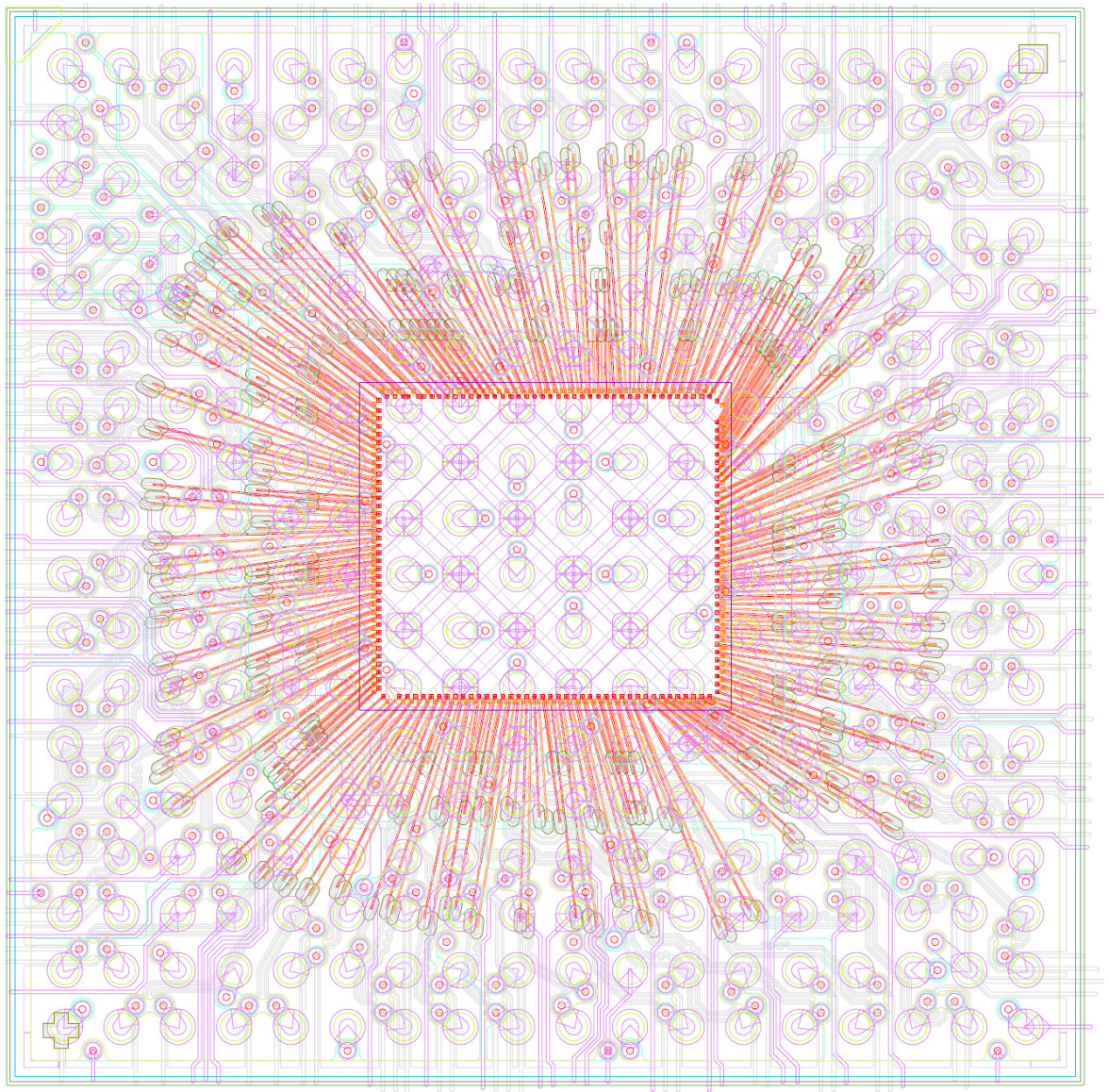
FILE NAME: 026956Epod–A_00

Package Connections of the FPGA (ball positions an Signal names)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	GND	SER_TX_N	SER_TX_P	GND	IO_N1_A2	IO_N1_A3	VDD_N1	IO_N1_A6	IO_N1_A8	IO_N2_A1	IO_N2_A3	GND	IO_N2_A5	IO_N2_A7	IO_E2_B8	IO_E2_B7	IO_E2_A7	GND	A
B	SER_RX_P	SER_RTERM	VDD_SER_PLL	IO_N1_B0	IO_N1_B2	IO_N1_B3	GND	IO_N1_B6	IO_N1_B8	IO_N2_B1	IO_N2_B3	VDD_N2	IO_N2_B5	IO_N2_B7	IO_E2_A8	GND	VDD_E2	IO_E2_B6	B
C	SER_RX_N	VDD_SER	POR_ADJ	IO_N1_A0	IO_N1_B1	VDD_N1	IO_N1_B4	IO_N1_B5	IO_N1_B7	IO_N2_B0	IO_N2_B2	GND	IO_N2_B4	IO_N2_B6	IO_N2_B8	IO_E2_A5	IO_E2_B5	IO_E2_A6	C
D	GND	CLK	TST	RST_N	IO_N1_A1	GND	IO_N1_A4	IO_N1_A5	IO_N1_A7	IO_N2_A0	IO_N2_A2	VDD_N2	IO_N2_A4	IO_N2_A6	IO_N2_A8	GND	IO_E2_B4	IO_E2_A4	D
E	CLK_B	GND	GND	VDD_CLK	VDD_PLL	GND	VDD_N1	GND	VDD_N1	GND	VDD_N2	GND	GND	VDD_N2	GND	VDD_E2	GND	VDD_E2	E
F	IO_W2_B7	IO_W2_A7	IO_W2_A8	IO_W2_B8	GND		GND	VDD_N1	GND	VDD	GND	VDD_N2		GND	IO_E2_A2	IO_E2_B2	IO_E2_B3	IO_E2_A3	F
G	IO_W2_B5	IO_W2_A5	IO_W2_A6	IO_W2_B6	VDD_W2	GND	VDD	GND	VDD	GND	VDD	GND	VDD_E2	VDD_E2	IO_E2_A0	IO_E2_B0	IO_E2_B1	IO_E2_A1	G
H	GND	VDD_W2	GND	VDD_W2	GND	VDD_W2	GND	VDD	GND	VDD	GND	VDD	GND	GND	IO_E1_A7	IO_E1_B7	IO_E1_B8	IO_E1_A8	H
J	IO_W2_B3	IO_W2_A3	IO_W2_A4	IO_W2_B4	VDD_W2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	VDD_E1	IO_E1_A5	IO_E1_B5	IO_E1_B6	IO_E1_A6	J
K	IO_W2_B1	IO_W2_A1	IO_W2_A2	IO_W2_B2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	GND	VDD_E1	GND	VDD_E1	GND	K
L	IO_W2_B0	IO_W2_A0	IO_W1_A8	IO_W1_B8	VDD_W1	GND	VDD	GND	VDD	GND	VDD	GND	VDD_E1	GND	IO_E1_A3	IO_E1_B3	IO_E1_B4	IO_E1_A4	L
M	IO_W1_B7	IO_W1_A7	IO_W1_A6	IO_W1_B6	VDD_W1	VDD_W1	GND	VDD	GND	VDD	GND	VDD	VDD_S2	VDD_E1	IO_E1_A1	IO_E1_B1	IO_E1_B2	IO_E1_A2	M
N	IO_W1_B5	IO_W1_A5	IO_W1_A4	IO_W1_B4	GND		VDD_S3	GND	VDD	GND	VDD_S1	GND		VDD_S2	IO_E1_A0	IO_E1_B0	IO_S2_B8	IO_S2_A8	N
P	GND	VDD_W1	GND	VDD_W1	IO_W1_B3	GND	GND	VDD_S3	GND	VDD_S1	GND	VDD_S1	VDD_S2	GND	IO_S2_A6	IO_S2_B6	IO_S2_B7	IO_S2_A7	P
R	IO_W1_B2	IO_W1_A2	IO_W1_B1	IO_W1_A1	IO_W1_A3	VDD_S3	JTAG_TCK	SPI_D1	IO_S1_A0	IO_S1_A2	VDD_S1	IO_S1_A4	IO_S1_A6	IO_S2_A0	IO_S2_A2	GND	VDD_S2	GND	R
T	IO_W1_B0	IO_W1_A0	CFG_MD0	CFG_MD1	JTAG_TDI	GND	SPI_FWD	SPI_D0	IO_S1_B0	IO_S1_B2	GND	IO_S1_B4	IO_S1_B6	IO_S2_B0	IO_S2_B2	IO_S2_A4	IO_S2_B4	IO_S2_B5	T
U	CFG_MD2	CFG_MD3	VDD_S3	GND	JTAG_TMS	VDD_S3	SPI_D2	SPI_CLK	IO_S1_B1	IO_S1_B3	VDD_S1	IO_S1_B5	IO_S1_B7	IO_S1_B8	IO_S2_B1	GND	VDD_S2	IO_S2_A5	U
V	GND	CFG_FAILED_N	CFG_DONE	POR_EN	JTAG_TDO	GND	SPI_D3	SPI_CS_N	IO_S1_A1	IO_S1_A3	GND	IO_S1_A5	IO_S1_A7	IO_S1_A8	IO_S2_A1	IO_S2_A3	IO_S2_B3	GND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

„X-ray vision“ of FPGA (Die in Package)



Packaged Sample from MPW-Run

Thank You for Your Attention!